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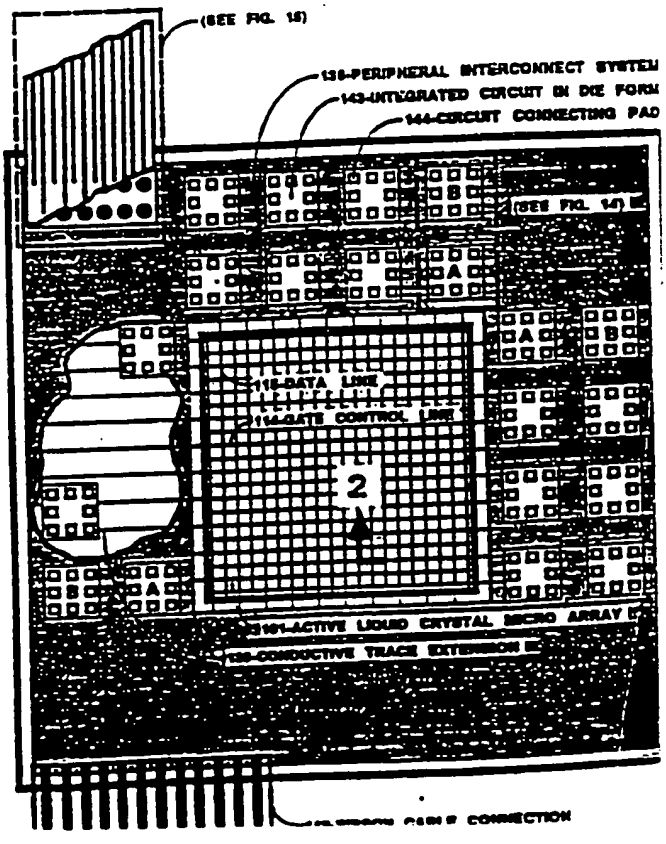
(54) Title: PROGRAMMABLE MASKING APPARATUS

(57) Abstract

An electronically programmable masking device (162) for photolithography applications, comprising an active liquid crystal micro array of programmable pixels (101), an interconnection system (138) and, in most embodiments, the drive and interface circuitry. The programmable pixels (101) can be electronically controlled to be opaque or transparent to the exposure light used in photolithographic exposure systems. The pixel (124) size must be such that when the pixel (124) is imaged on the target surface, the resulting size is compatible with the pattern resolution required on the target surface. The space between pixels (124), referred to as the pixel gap (106), must be of a size such that it cannot be resolved by the optics (162, 166) of the exposure system. A communications link provides for direct downloading of patterning data to the device from external sources such as computer aided design (CAD) systems.



# Specification
# "PROGRAMMABLE MASKING APPARATUS"

## FIELD OF THE INVENTION

This invention relates generally to a programmable masking apparatus and more particularly to a liquid crystal based, electronically programmable high resolution masking device and method for use in conjunction with image generation and image transfer systems.

A specific application of the present invention relates to programmable masking devices for use in conjunction with exposure systems for the purpose of generating photolithographic images on photosensitive surfaces.

An even more specific application of the present invention relates to programmable reticles or masks for use in conjunction with ultraviolet exposure systems in the photolithographic processes associated with semiconductor manufacturing. In this specific application of the present invention, such programmable reticles or masks utilize a liquid crystal micro-array of programmable pixels to define the desired opaque and transparent patterns of the reticles or masks.

## DESCRIPTION OF PRIOR ART

Photolithographic pattern generation relies mostly on optical exposure systems which transfer fixed patterns, previously defined on masking devices, to photosensitive target surfaces in the form of latent images. Such photolithographic pattern generation is widely used in the industry in large volume processes requiring pattern replication.

A major application of this technology is found in the semiconductor industry where such masking devices typically consist of glass or quartz substrates wherein the desired patterns are defined on hard surface films such as chrome or iron oxide. These

films must be opaque to the ultra violet light required for the operation of the wafer exposure systems used in the microlithography of semiconductor wafers. In this application, such masking devices are used in two distinct configurations. In the first configuration, known as a mask, the masking device comprises a large number of identical patterns, where each pattern corresponds to a semiconductor device or circuit. In the second configuration, known as a reticle, the masking device typically comprises the patterns corresponding to one integrated circuit. Masks are used with wafer exposure systems which transfer the mask patterns to a wafer surface in a single operation. Reticles are used with wafer exposure systems known as wafer steppers which transfer the pattern on the reticle to a large number of sites on the wafer by sequentially stepping from site to site and repeating the exposure operation at each site.

In accordance with present technology, these masks and reticles are typically fabricated with electron beam writing systems which, by means of photolithographic techniques, translate computer aided design (CAD) data into permanent patterns on the surface of the transparent substrate.

The complete wafer fabrication process for each specific device or integrated circuit requires a set of masks and/or reticles which comprises all the patterning layers required by the specific fabrication process. Depending upon technology, the number of these layers may vary from a few, for very simple processes, to approximately 30 for very complex processes, with 12 to 16 being typical for most integrated circuit process technologies.

Masks and reticles currently range in cost from $400 to over $1,500 and typically take two weeks to obtain when ordered from commercial suppliers. In addition, integrated circuit layouts are often revised, requiring the generation of new sets of masks and/or reticles with each revision. As a result, wafer fabrication facilities are often burdened with substantial mask and reticle inventory costs. Further, the delays associated with the introduction of new masks and/or reticles delay the introduction of new products and product improvements, severely limiting potential profitability.

To perform the photolithographic processes of semiconductor fabrication, the masks and/or reticles are installed in exposure systems and must be frequently changed

to accommodate the production requirements of a large combination of layers an products. These frequent changes result in substantial setup time penalties, causing reduction in productivity of the associated exposure systems, which normally range i cost from $500,000 to over $1,000,000 each.

For several years the semiconductor industry has been searching for cost effectiv means of directly translating, in real time, computer aided design (CAD) data int patterns on the wafers. Direct electron beam writing systems can technically perform this task. However, their costs are in the millions of dollars and their throughputs ar limited to a few wafers per hour compared to 30 to 60 wafers per hour for ultra viole exposure systems. These constraints make direct electron beam writing a cos ineffective technology for wafer manufacturing. To date, the practical use of such direct electron beam writing systems has been limited to research projects and to th commercial production of masks and reticles for use in conjunction with ultraviole exposure systems.

The conventional technology which is based upon the use of fixed masks an reticles in conjunction with ultra violet exposure systems has proven to be a cos effective technology in producing semiconductor products in large volume. However, suffers from a number of disadvantages, most significantly:

(a) The inability to image directly onto a wafer surface, patterning data provide by a computer system, thereby seriously impairing the evolution of custor integrated circuit technologies and wafer scale integration. Wafer scal integration, is a technology outlined in further detail under the sectio covering the objects and advantages of the present invention.

(b) The requirement for maintaining and managing large inventories of masks an reticles to support a typical wafer fabrication facility.

(c) The substantial expenditures associated with the continuing need to genera new masks and reticles to support product updates and improvements.

(d) The additional two week typical delay in the introduction of new produc

and product ovements resulting from the time necessary for the generation of ne masks and reticles.

(e) The productivity losses due to the setup times associated with the frequent changes of masks and reticles which are typically required in the course of the normal operation of a wafer processing facility.

(f) The inability to support pattern repair process technology. Such technology could provide the means for achieving substantial yield increases in the manufacture of semiconductor devices.

The use of liquid crystal technology for the purposes of producing programmable photolithographic masking devices has been very limited. However U.S. Pat. No.4,653,860, issued on March 31, 1987, describes the use of a programmable liquid crystal shutter inserted in the light path of a direct wafer stepper to selectively illuminate, under remote control, specific areas of a hard surface reticle. Unlike the current invention, this device does not operate directly as a high resolution programmable patterning system. Rather, the patterns are defined by a conventional hard surface reticle which provides the desired image resolution and the illumination is selectively controlled by a liquid crystal shutter inserted in the light path. As stated in that patent its field of applicability is limited to those applications requiring minor programming changes whereby the major portion of the reticle remains unchanged for the various programming options required.

## OBJECTS AND ADVANTAGES OF THE INVENTION

The general object of the present invention is to provide electronically programmable high resolution masking devices.

Such programmable masking devices will use liquid crystal technology to define an electronically programmable micro array of pixels. The optical resolution of these devices will be compatible with the specific requirements of each application. The pixels can be individually programmed to be transparent or opaque to the light used in

conjunction with each specific type of application of the present invention. Driving circuitry will control the rows and columns of such micro array, providing the capability of applying the appropriate control voltage to each pixel as means of defining the desired patterns. A bit map micro array memory will store the pattern data which is conveyed to the pixels via the driving circuitry. Interface circuitry will be incorporated enabling computer systems to communicate with the micro array memory in both the read and write modes.

Another general object of the present invention is to provide electronically programmable high resolution masking devices for use in conjunction with image transfer systems, as means for implementing direct imaging of computer generated patterning data onto photosensitive substrates or surfaces.

Still another object of the present invention is to provide programmable reticles and masks which can be integrated into the ultraviolet exposure systems used in semiconductor manufacturing, for the purposes of implementing, in real time, direct imaging of pattern generation data onto the surface of semiconductor waters.

Further objects and advantages of such programmable reticles and masks are:

(a) To provide a means of converting pattern generation data, directly into liquid crystal micro array patterns which will appear in the optical plane normally occupied by conventional masks or reticles, when such masks or reticles are mounted in ultraviolet exposure systems in the proper position for the exposure of wafers.

(b) To provide means for downloading pattern generation data directly from a computer system into such programmable masks and reticles.

(c) To provide means for the efficient fabrication of fully customized integrated circuits with relative costs and fabrication times comparable to those of commercial integrated circuits. This object can be achieved by the use of the present invention to translate computer aided design (CAD) data into patterns

(d) To eliminate the intermediate process step through which fixed masks and reticles are typically generated.

(e) To eliminate the inventory costs of masks and reticles typically associated with the conventional masks and reticles presently used in semiconductor manufacturing.

(f) To improve the productivity of expensive ultraviolet exposure systems by eliminating the setup times typically associated with conventional masks and reticles.

(g) To provide means for repairing defects which may have been detected, during the various inspections performed on the patterns produced on the wafer surface. Such inspections, are typically performed after photoresist image definition (in-process inspection) and after the completion of all the steps which constitute a complete photolithographic process sequence (final inspection). Such pattern repair may be accomplished with the use of the present invention by defining, in real time, an appropriate repair pattern based upon defect data collected during inspection. Such repair pattern would then be used in conjunction with an appropriate pattern repair process for the purpose of repairing defective patterns identified during inspection.

(h) To provide wafer stepper exposure systems with the capability of changing critical dimensions and patterns from field to field to facilitate circuit performance optimization, yield enhancement and process improvement.

(i) To substantially reduce the cycle time required for the development and introduction of new integrated circuits.

(j) To provide wafer stepper exposure systems with the capability of printing different products on the same wafer by changing the reticle pattern under computer control while the exposure system steps from field to field.

(k) To provide a cost effective approach for the implementation of wafer scale integration. Wafer scale integration refers to the creation of a complete electronic system on a silicon wafer, involving the three fundamental technologies outlined below:

1. The technology to produce on the same wafer all the different types of integrated circuits required for a complete electronic system. This technology can be implemented by the use of the present invention as outlined above.

2. The technology to identify through test procedures all the functional integrated circuits of each type on the same wafer. This technology is currently available in the industry.

3. The technology to generate, in real time, an appropriate interconnect pattern to produce a complete electronic system out of functional integrated circuits available on the same wafer. This technology can be implemented by the capability of the present invention to translate, in real time, computer aided design (CAD) data into interconnect patterns printable directly onto the wafer surface.

Additional objects of the present invention are to provide electronically programmable high resolution masking devices for use in visual display projection systems, real time holography, printing systems and other applications requiring the high resolution and programmability of the present invention.

## DESCRIPTION OF THE DRAWINGS

In the drawings, which form an integral part of the specification of the present invention and which are to be read in conjunction therewith, and in which like reference numerals are employed to designate similar components in various views:

**Fig. 1** is a simplified plan view depicting the principal components of a preferred embodiment of the present invention;

**Fig. 2** is a representational partial cross section taken along the line 2-2 in Fig. 1 depicting a portion of an active liquid crystal micro array and the peripheral circuitry associated with it;

Fig. 3 is a pictorial representation of the conductive coatings which serve as pixel electrodes for the active liquid crystal micro array shown in Fig. 1;

Fig. 4 is a representational partial top plan view illustrating the configuration of the active liquid crystal micro array shown in Fig. 1;

Fig. 5 is a representational partial cross section taken along the line 5-5 in Fig. 4 illustrating the configuration of one of the transistor switches used in the active liquid crystal micro array;

Fig. 6 is a pictorial representation of the micro array interconnection system comprising control lines, data lines, transistor switches and pixel electrodes in accordance with the present invention;

Fig. 7 is a representational partial plan view depicting the common electrode, pixel electrodes, gate control lines and data lines of the preferred embodiment;

Fig. 8 depicts two alternative configurations for the common electrode of Fig. 7 comprising (1) the addition of orthogonal metal traces to lower the sheet resistance of this electrode and (2) the addition of red (R), green (G) and blue (B) color filters for digital color imaging.

Fig. 9 is a representational partial cross section taken along the line 9-9 in Fig. 8, to further illustrate the orthogonal metal traces;

Fig. 10 is a representational partial top plan view similar to that shown in Fig. 4 with the exception of the transistor switches which are configured with redundant terminals, depicting an alternate embodiment of the present invention;

Fig. 11 is a representational partial cross section taken along the line 11-11 in Fig. 10 showing a redundant field effect transistor switch with one source, two gates and two drains;

Fig. 12 is a representational partial top plan view illustrating a temporary interconnection system used for testing the integrity of the transistor switches associated with each of the pixels in the micro array;

Fig. 13A is a representational partial cross section illustrating a defect on the first layer metal of a redundant double layer metal interconnecting system;

Fig. 13B is a representational partial cross section illustrating a defect on the second layer metal of a redundant double layer metal interconnecting system;

Fig. 14A is a representational partial top plan view illustrating the principle for the dual layer interconnecting system according to one of the proposed embodiments of the present invention;

Fig. 14B is a representational partial top plan view illustrating a preferred configuration of the peripheral interconnect system comprising three layers of metalization;

Fig. 15 is a representational partial top plan view illustrating a contactless connector system used in accordance with the present invention and comprising infrared transmitters and receivers;

Fig. 16 is a representational partial cross section taken along the line 16-16 in Fig. 15 showing the configuration of the contactless connector system illustrated in Fig. 15;

Fig. 17 is a simplified schematic diagram illustrating one of the preferred circuits used to control the voltage applied to each pixel as means of modulating its transparency;

Fig. 18 is a pictorial representation of a photolithographic exposure apparatus illustrating the use of the programmable masking device of the present invention to generate images on a photosensitive target surface from data provided by a computer system;

Fig. 19 is a pictorial representation illustrating the use of the programmable masking device of the present invention in a visual display projection system;

Fig. 20 is a pictorial representation illustrating the use of the programmable masking device of the present invention in a three dimensional projection viewing system;

Fig. 21 is a pictorial representation illustrating the use of the programmable masking device of the present invention in a holographic imaging apparatus;

Fig. 22 is a pictorial representation illustrating the use of the programmable masking device of the present invention in a printing apparatus.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Various embodiments of the present invention are described in this section starting with the embodiment with the simplest configuration which, for convenience, will be designated as the first embodiment. The description of this first embodiment is followed by an analysis of the technological problems associated with the implementation of the present invention. This analysis serves as the background for the improvements and features comprised in other embodiments described in this section which, for convenience, will be designated as second, third and fourth embodiments. Next, the issue of connectivity to an external computer system is addressed. This issue is followed by the description of a fifth embodiment which provides the capability of modulating the transparency of each pixel in the micro array. Then, there are some considerations related to special applications of the present invention to semiconductor manufacturing and finally two procedures are described, designated as test procedure and alternate interconnection procedure. These procedures overcome yield limitations in the manufacture of the embodiments described, thus providing cost effective means for commercially producing such embodiments.

Fig. 1 is a simplified plan view depicting the most relevant elements comprised in the preferred embodiments of the present invention. These elements are not necessarily included in each of these embodiments but are incorporated in this figure for reference in the descriptions which follow. This figure shows the active liquid crystal micro array **101** which is fully described in the first embodiment and represents the key element of the present invention. Within the micro array this figure shows the gate control lines **114** which must be sequentially enabled to provide a control voltage, via the data lines **115**, to each pixel in the micro array. The area surrounding the micro array provides space for the peripheral interconnect system **138** which is described in the fourth embodiment. This peripheral interconnect system comprises the integrated circuits in die form **143**, other interconnections shown in further detail in **Fig. 14A** and the conductive trace extensions **139** which are the extensions of the gate control lines and the data lines. Also depicted are the locations of the integrated circuit connecting pads **144**, a ribbon cable connection **149** and an alternate contactless electronic connector described in detail in **Fig. 15**.

**The first embodiment**

**The first embodiment of the present invention** will be described with additiona reference to figures 2 through 9.

**Fig. 2** is a representational partial cross section taken along line 2-2 in Fig. 1 depicting a portion of an active liquid crystal micro array and the peripheral circuitry associated with it. The structural elements of the peripheral interconnect system pertain to the **fourth embodiment of the present invention** and their description is covered in detail in that section.

This first embodiment of the present invention comprises a glass primary substrate **102** and a glass secondary substrate **103**, both bonded to a thin perimeter spacer **109** which holds the substrates in close proximity and parallel to each other. The volume delimited by these two parallel substrates and the perimeter spacer forms a sealed chamber containing a liquid crystal material **108**.

Each of the substrates is coated, on the inner side of the chamber, with a thin conductive transparent film such as aluminum or indium tin oxide. These conductive films are used to define the electrodes necessary for the operation of the liquid crystal. On the primary substrate **102** the coating is patterned to form a micro array of discrete pixel electrodes **104** organized in rows and columns. On the secondary substrate **103** the coating is continuous and forms the common electrode **105**. This electrode encompasses an area equivalent to the entire micro array area defined on the primary substrate **102**. The space between adjacent pixel electrodes is called the pixel gap **106**. The areas defined by the pixel gaps **106** are used to locate the transistor switches **107** by means of which the desired control voltages are applied to each of the pixel electrodes **104**.

The primary substrate **102** and the secondary substrate **103** are both coated on the outer side of the chamber with a polarizing film shown in **Fig. 2** as the primary substrate polarizer **202** and the secondary substrate polarizer **203**. These polarizing films are oriented such that the polarization angle between them is 90 degrees, thereby insuring that no light can be transmitted through both polarizing films when the

polarization angle is not rotated by the liquid crystal material 108.

Fig. 3 is a perspective representation of the conductive coatings which serve as pixel electrodes for the active liquid crystal micro array of Figs. 1 and 2. It shows the pixel electrodes 104, the common electrode 105 and the pixel gaps 106. The area encompassed by the pixel gaps of the entire micro array forms a set of rows and columns with a width equal to the pixel gap 106. This area is used to locate the active electrical components and the interconnection system required for the operation of the liquid crystal micro array. The interconnection system incorporates a set of conductive traces which are extended towards the periphery of the micro array and are shown in several of the figures herein as the conductive trace extensions 139 (see Fig. 1). These traces provide the electrical connections between the pixel electrodes 104 and the control circuitry.

The above configuration is similar to that found in some active matrix liquid crystal displays. However, it differs with regards to the pixel size, the pixel gap and other features applicable to the various embodiments of the present invention.

Fig. 4 is a representational partial top plan view illustrating the configuration of the active liquid crystal micro array shown in Fig. 1. In the preferred embodiments of the present invention, the active electrical components are MOS thin film transistors made of polycrystalline silicon, commonly known as polysilicon. However, other semiconductor materials and device structures could be used in different embodiments.

As shown in this figure, the polysilicon is patterned in rectangular islands 110 laying along the columns of pixel gaps 106. As an alternative, the polysilicon could be patterned in long strips covering the entire length of the columns of pixel gaps 106. The MOS transistors are configured with the control gate area 111 of each transistor in line with a row of pixel gaps 106. This configuration offers a simple layout where the gate control lines 114 are straight metal traces patterned over the rows of pixel gaps 106, thus creating a common gate electrode for all the MOS transistors in a row . The other two electrodes of the MOS transistor, known as the source and the drain, are patterned as a source contact 112 and a drain contact 113 to the polysilicon material. These electrodes are located on opposite ends of the rectangular polysilicon island 110.

and the drain contact is connected to a metal trace forming a data line 115 patterned over the column of pixel gaps which the transistor is located.

Fig. 5 is a representational partial cross section taken along the line 5-5 in Fig. 4 illustrating the configuration of one of the transistor switches used in the active liquid crystal micro array. The cross section shows the structure of the MOS transistor with the source 118 and the drain 117 formed in the polysilicon island 110. The pixel tab 116 is patterned over the source contact 112 and the data line 115 is connected to the drain contact 113. The gate structure is formed by the oxide 119, which is thermally grown over the polysilicon island 110. The cross section also shows that the data line 115 which runs over the polysilicon islands along the columns of pixel gaps is electrically isolated from the underlying structures by the dielectric 120.

Fig. 6 is a pictorial representation of the active matrix interconnection system comprising the control lines 114, the data lines 115, the transistor switches 121 and the pixel electrodes 104. It further illustrates, in schematic form, the configuration of the interconnection system through which control voltages are applied to the pixel electrodes. As shown, the pixel tab 116 of each pixel electrode 104 is connected to a data line 115 via a simulated transistor switch 121. The trace on a specific row is connected to the control gates of all the transistor switches 121 on that row and becomes a gate control line 114. The trace on a specific column is connected to the other electrode of all the transistor switches 121 on that column and becomes a data line 115. Also shown are the pixel gaps 106.

Fig. 7 is a representational partial plan view depicting the common electrode 105, the pixel electrodes 104, the gate control lines 114 and the data lines 115 which are shown with an interdigitated layout. As shown in this figure, the configuration described above offers a simple layout where the gate control lines 114 and the data lines 115 are straight metal traces patterned over the rows and columns of pixel gaps. Both of these sets of traces are extended beyond the edge of the micro array of pixels to an area where it is practical and feasible to create electrical connections to the drive circuitry which controls the electronic state of each pixel. In this figure, the data lines 115 are depicted with interdigitated extensions, whereas the gate control lines 114 are depicted with non interdigitated extensions. The common electrode 105, deposited on

the secondary substrate and shown on a higher plane, in this figure, is connected to a perimeter trace 122 which is patterned around the perimeter of the common electrode 105. In turn, this perimeter trace is connected to the electrical ground of the primary substrate interconnection system. Also shown in this figure, in a lower plane, are the pixel electrodes 104.

Fig. 8 depicts two alternative configurations for the common electrode 105 comprising (1) the addition of orthogonal metal traces to lower the sheet resistance of this electrode and (2) the addition of red (R), green (G) and blue (B) color filters for digital color imaging. This figure shows the common electrode 105 and the perimeter trace 122 described above.

The first alternative configuration comprises a set of orthogonal metal traces 123 deposited over those areas which match the rows and columns of pixel gaps on the primary substrate. These orthogonal metal traces divide the common electrode 105 into pixel areas 124 which match the pixel electrodes on the primary substrate. As a result the effective sheet resistance of the common electrode 105 will be substantially reduced causing the micro array to respond faster to the control signals which determine the state of each pixel.

This first alternative configuration can be further modified to provide a precise edge definition of each pixel. As described above, the complex structures built on the surface of the primary substrate may cause a minimum amount of pixel edge irregularities. Such irregularities will not be resolved by the image transfer optics of the exposure system and, therefore, will not impair the satisfactory operation of the device. However, for special applications, it may be desirable to provide a precise edge definition of each pixel. This may be achieved by making the width of these orthogonal metal traces slightly larger than the pixel gap and by using a metal such as chrome, which offers excellent edge definition, to generate the orthogonal metal traces.

The second alternative configuration comprises further the deposition of red (R) green (G) and blue (B) color filters over the pixel areas 124, as shown in Fig. 8, for applications of the present invention requiring color imaging.

Fig. 9 is a representational partial cross section taken along the line 9-9 in Fig. 8 to further illustrate the orthogonal metal traces 123. As shown, the conductive film which forms the common electrode 105 is deposited over the secondary substrate 103 and the orthogonal metal traces 123 are then deposited on the lower surface of the common electrode 105. The space between the metal traces 123 comprises the pixel areas 124 described above. Since the sheet resistivity of these metal traces is orders of magnitude lower than that of the conductive film which forms the common electrode 105, the effective sheet resistance of the common electrode 105 is substantially reduced by the addition of these orthogonal metal traces 123.

**Analysis of the technological problems associated with the implementation of the present invention.**

In order to produce an image of acceptable quality on the target surface, any embodiment of the present invention must satisfy two fundamental conditions:

(1) The pixel size in the micro array must be such that the resulting size of the pixel image on the target surface is compatible with the applicable pattern generation design rules. More specifically, the size of the pixel image on the target surface must be such that the minimum feature size dictated by the applicable pattern generation design rules will be equal to or will be a multiple of the size of the pixel image on the target surface.

(2) The width of the pixel gap in the micro array must be less than the minimum size which can be resolved by the image transfer optics of the photolithographic exposure system. This condition will insure that the patterns imaged on the target surface are free of gaps between adjacent pixels.

Compliance with these two conditions is a fundamental requirement for the proper operation of the present invention. Therefore, the pixel size and the width of the pixel gap, in any embodiment of the present invention, must be tailored to comply with the requirements dictated by the exposure system to be used and the minimum feature size to be produced.

Pixels in the micro array may have a variety of different shapes such as circular, triangular, rectangular, etc. and may be organized in a variety of different configurations such as a rectangular array, a polar array or other suitable configuration. However, most practical implementations of the present invention will use a rectangular array of square pixels compatible with the elemental cell of typical computer aided design (CAD) systems.

The second, third and fourth embodiments of the present invention pertain to applications requiring very high density micro arrays, where the number of pixels in the micro array may range from 100 million to over one billion. Such types of applications will be found in the semiconductor industry as shown in the examples which illustrate the uses of the various embodiments described. When the number of pixels reaches the above values, the defect limited yields and the connectivity must be properly analyzed in order to establish the requirements for the practical and economical producibility of such embodiments. The example which follows will clearly illustrate these problems and will explain the solutions offered by the second, third and fourth embodiments of the present invention to address such problems.

Consider a micro array with the following characteristics:

* Array configuration: 15,000 by 15,000 pixels
* Pixel size: 4 microns by 4 microns
* Pixel gap: 1 micron
* Interconnect trace width: 1 micron
* Effective gate area: 1 micron square

Such micro array would comprise a total of 225 million pixels and encompass an area approximately 7.5 by 7.5 centimeters square. The total equivalent area occupied by all the gates in the micro array would correspond to approximately 2.25 square centimeters and the total equivalent area occupied by all the interconnect traces within the system, including the conductive trace extensions, would correspond to approximately 22.5 square centimeters.

be achieved. On the basis of this defect density, the first embodiment of the present invention would have a high probability of exhibiting at least one defect in the control gate of one of the transistor switches, and at least eleven defects in the interconnect system metal traces. Since these programmable masking devices must be defect free, the first embodiment, described above, are not recommended for applications requiring very high density micro arrays.

Connectivity also presents a technological difficulty. In the example above, the micro array would have two orthogonal sets of metal traces. Each set would comprise 15,000 traces, one micron wide, with four micron spaces between two adjacent traces. The connection of these traces to the drive circuitry via any type of cabling system would be clearly impractical if not impossible to implement, making the first embodiment of the present invention, described above, undoable for this type of application.

The basic problems, presented above, are successfully addressed by the second, third and fourth embodiments of the present invention described below.

The second embodiment

The second embodiment of the present invention is described with reference to figures 10, 11 and 12. This embodiment is configured with double transistor switches to address the gate area integrity problem discussed above.

Fig. 10 is a representational partial top plan view similar to that shown in Fig. 4 with the exception of the transistor switches which are configured with redundant gate and drain terminals. Like Fig. 4, this figure shows the pixel electrodes 104 connected to the source contact 112 of the transistor switch, via the pixel tab 116. However, the transistor switches in this second embodiment are configured with two control gates and two drain contacts shown in this figure as the primary control gate 125, the primary drain contact 126, the secondary control gate 127 and the secondary drain contact 128. As explained in further detail below, these secondary electrodes are used to replace the primary electrodes when the presence of a defect in the primary control gate causes the transistor switch to malfunction. When [illegible]

gate 125, the secondary control gate 127 is connected to the gate control line 114 by a metalization patch shown as the secondary control gate connection 129. The procedure for applying this metalization patch is described in detail under the special test and repair procedure at the end of this section. Also shown in this figure are the data lines 115, the pixel gaps 106 and the polysilicon islands 210, all of which have been explained with reference to Fig. 4.

Fig. 11 is a representational partial cross section taken along the line 11-11 in Fig. 10 showing a redundant field effect transistor switch with one source, two gates and two drains. The cross section shows the structure of the redundant MOS transistor with the source 118, the primary drain 130 and the secondary drain 131 formed in the polysilicon island 210. Like in Fig. 4, the pixel tab 116 is patterned over the source contact 112. However the data line 115 is shown connected to the secondary drain contact 128 rather than the primary drain contact 126. This figure is intended to illustrate the secondary control gate connection 129 connecting the secondary control gate 127 to the gate control line 114. When the primary control gate 125 is found to be defective, this alternate connection is made in its place. The cross section also shows the thermal oxide 119 and the dielectric 120 which have previously described with reference to Fig. 4.

Fig. 12 is a representational partial top plan view illustrating a temporary interconnection system used for testing the integrity of the transistor switches associated with each of the pixels in the micro array. Each polysilicon island 210 has one source contact 112, a primary control gate 125, a primary drain contact 126, a secondary control gate 127 and a secondary drain contact 128. The temporary interconnection system comprises a set of temporary source test lines 132 and a set of temporary drain test lines 133. Each temporary source test line 132 is connected to the source contact 112 of each of the transistor switches adjacent to that line and each temporary drain test line 133 is connected to the primary drain contact 126 of each of the transistor switches adjacent to that line. Like for normal operation, each gate control line 114 is connected to the primary control gate 125 of each transistor in the row associated with that gate control line. With this temporary interconnection system every transistor switch in the micro array can be individually tested for functional integrity. The [illegible] and the secondary drain contacts 128 are not connected

during this test procedure. All gate control lines 114, temporary source test lines 132 and temporary drain test lines 133 are terminated on probing pads providing electrical access to these interconnections.

If a primary control gate is found to be defective, as determined by test procedures such as those outlined at the end of this section, alternate connections are made in place of their primary counterparts. The secondary control gate 127 is connected to the gate control line 114 via the alternate gate connection 227 and the secondary drain contact 128 is connected to the temporary drain test line 133 via the alternate drain connection 228. Fig. 12 also depicts the defective gate area 225 and the primary drain link 226 explained with reference to an alternate interconnection procedure used to modify these metal interconnections which is outlined at the end of this section . This procedure is an integral part of the technology required for the production of the various embodiments of the present invention.

The third embodiment

The third embodiment of the present invention is described with reference to figures 13A and 13B. This embodiment is identical to either of the previously described embodiments except that it is configured with two layers of metal traces directly applied over each other as a means of circumventing the metal trace discontinuities generated by photolithographic defects.

Fig. 13A is a representational partial cross section illustrating a defect on the first layer metal of a redundant double layer metal interconnecting system. It depicts the second layer metal 135 directly superimposed over the first layer metal 134 and a typical defect on the first layer metal 136.

Fig. 13B is a representational partial cross section illustrating a defect on the second layer metal of a redundant double layer metal interconnecting system. It also depicts the second layer metal 135 directly superimposed over the first layer metal 134 and a typical defect on the second layer metal 135.

These two layers of metal are independently patterned in order to statistically

insure that defects on one layer do not coincide with defects on the other layer. Electrical continuity of the control lines and the data lines is therefore assured and the integrity of the interconnection system is properly safeguarded.

An alternative to this dual layer metal interconnect system is a single layer metal interconnect system used in conjunction with the pattern repair technology outlined under the section describing the objects and advantages of the present invention. This technology can be used to repair the typical defects which would normally occur during patterning of the metal interconnection system. Missing metal may be repaired by selectively depositing a bridging metal trace over each metal discontinuity. Excess metal may be removed by selectively removing the excess metal.

The fourth embodiment

The fourth embodiment of the present invention is described with reference to figures 2, 14A and 14B. This embodiment is configured with a double layer metalization system on the periphery of the micro array. This peripheral metalization system provides the space and the interconnections necessary to incorporate the drive and interface circuitry on the surface of the primary substrate. At the same time, the control lines and the data lines are extended beyond the periphery of the micro array to the outer edge of the peripheral metalization system and become an integral part of this system. The configuration of this fourth embodiment, incorporating the drive and interface circuitry as integral parts of the programmable masking device, circumvents the connectivity problems presented above by eliminating the need for any type of cabling connections between the micro array and the drive circuitry.

As previously indicated, Fig. 2 is a representational partial cross section taken along line 2-2 in Fig. 1 depicting a portion of the active liquid crystal micro array and the peripheral circuitry associated with it. The structural elements of the active liquid crystal micro array have already been described with reference to the first embodiment of the present invention and need not be repeated. The structural elements of the peripheral interconnect system are associated with the fourth embodiment of the present invention and are described in this section. The right side of Fig. 2 shows the

metalization traces 142, are isolated from the conductive trace extensions 139, by a dielectric isolation layer 141. The intermetallization connection 140 establishes the electrical connection between the conductive trace extensions 139 and the second metalization 142. Also shown are the integrated circuits in die form 143 connected to the second metalization 142.

Fig. 14A is a representational partial top plan view illustrating the layout principle for the dual layer interconnecting system used in this fourth embodiment of the present invention. It depicts the conductive trace extensions 139, the second metalization traces 142, the intermetallization connections 140 and the circuit connecting pads 144. The first set of pads labeled A 145 is connected, via the second metalization traces 142 and the intermetalization connection 140, to the first group of traces 146 of the conductive trace extensions 139. The second set of pads labeled B 147 is connected, via the second metalization traces 142 and the intermetalization connection 140, to the second group of traces 148 of the conductive trace extensions 139. This configuration is continued with additional groups of traces connected to additional sets of pads located in the area extending towards the periphery of the primary substrate. This layout overcomes potential spacial constraints and provides the necessary space for all of the conductive trace extensions 139 to be connected to the appropriate circuit connecting pads 144. These circuit connecting pads 144 are used to accept the connection to the integrated circuits in die form as shown in Fig. 2. Such pads may also be used as probing pads to test the integrity of the transistor switches in the micro array in accordance with the special test procedures outlined below.

Fig. 14B shows a variation of this embodiment configured with a three layer metalization system, where the first layer is formed by the conductive trace extensions 139, the second layer is formed by the second metalization traces 142 and the third layer comprises the circuit connecting pads 144. With this configuration, the metal traces on the second layer lie on a plane which is separated by a layer of dielectric from the plane containing the circuit connecting pads. The addition of the third metalization layer, as shown in Fig. 14B, removes the constraint that the traces of the second metalization must be placed around the area covered by the circuit connecting pads. Such traces can now be routed in the areas beneath the circuit connecting pads, thus providing improved utilization of the space available for interconnections and

increasing the packing density of the interconnect system. This configuration further allows the circuit connecting pads to be extended to encompass a circuit connection area 244 and a probing area 344 as illustrated in Fig. 14B. This three layer metalization will be specifically recommended for programmable masking devices with more than 256 million pixels which will require a higher packing density for the drive and interface circuitry.

**Connectivity to an external computer system**

The operation of the active matrix micro array, which is the object of the present invention, relies upon the capability of establishing the required electrical connections between the conductive trace extensions and the drive circuitry and further between the drive circuitry and an external computer system. When the number of conductive trace extensions does not exceed 1000, direct ribbon cable connections, similar to those used in liquid crystal displays can be successfully implemented in manufacturing. However, when the number of conductive trace extensions substantially exceeds 1000, such connections would be very difficult if not impossible to successfully implement.

For those applications of the present invention requiring that many conductive trace extensions, the fourth embodiment of the present invention, described above provides a viable solution since it eliminates the requirement for such connections.

Still to be addressed, is the problem of connectivity between the drive circuitry and an external computer system to be used in conjunction with the present invention. This problem is less severe than the connectivity between the conductive trace extensions and the drive circuitry since, in this case, the total number of interconnecting lines would not exceed 256 under the worse possible circumstances. A connection with this limited number of lines can easily be implemented, as shown in Fig. 1, with the ribbon cable connection 149. As an alternative, a contactless data communication connector system physically attached to the primary substrate can be used, as shown in Fig. 1, and described in detail with reference to figures 15 and 16.

Fig. 15 is a representational partial top plan view illustrating a contactless connector system comprising a set of collimated infrared transmitters and receivers

Interconnect traces 153 patterned over the primary substrate 102, establish the electrical connection between the interface circuitry and dual sets of infrared transmitters 150 and infrared receivers 151. On the connector body 152 which is physically separated from the primary substrate 102, there are matching sets of infrared transmitters 150 and infrared receivers 151 together with their respective interconnect traces 153.

Fig. 16 is a representational partial cross section taken along the line 16-16 in Fig. 15 showing the configuration of the contactless connector system illustrated in Fig. 15. It shows the primary substrate 102 physically separated from the connector body 152, and shows their respective infrared transmitters 150 and infrared receivers 151.

When the programmable masking device is installed in an exposure system, the infrared transmitters and receivers will be aligned with a matching set of receivers and transmitters mounted in the exposure system. With this configuration, there is no physical contact between the two sets of transmitters and receivers and, as a result, the programmable masking device is provided with a stress free data communications infrared link. This feature will be significant in applications, such as semiconductor microlithography, where the alignment of the programmable masking device must be held within a fraction of a micron.

## The fifth embodiment

The fifth embodiment of the present invention is described with reference to figure 17. This embodiment is substantially the same as the fourth embodiment described above with the addition of special circuitry to individually control the voltage level applied to each of the pixels in the micro array as means of modulating the relative transparency of each pixel.

Fig. 17 is a simplified schematic diagram illustrating one of the preferred circuits used to control the voltage applied to each pixel as means of modulating its transparency. It shows a group of N data lines 115 connected to the outputs of a 1 to N analog switch 158. The input of the analog switch 158 is connected to the output of a digital-to-analog (DAC) converter 157 which generates the desired analog voltage to

memory 156. The DATA IN ports of this memory 156 are connected to a data bus 154 providing a data communications link to the computer system which controls the programmable micro array. An address bus 155 carries the required address information to the SELECT ports of both the N word memory 156 and the analog switch 158. The circuit of Fig. 17 is repeated for each group of N data lines as many times as necessary to cover all the data lines in the micro array. The same data bus 154 and address bus 155 provide the required data and address information to all of these circuits in accordance with the configuration shown in Fig. 17.

**Considerations related to special applications of the present invention.**

One of the most significant applications of the present invention will be as a programmable masking device for the ultraviolet exposure systems used in semiconductor microlithography. For this specific type of application, any embodiment of the present invention must further comply with the following constraint:

The liquid crystal material, the two substrates and the conductive coatings must offer a combined level of transparency to ultraviolet light compatible with the requirements of the specific exposure system to be used in the photolithographic processes.

For the longer wave lengths, in the 340 to 470 nanometer range, such substrates can be made of high quality glass of the type used for semiconductor photolithography masks. For the shorter wave lengths, in the 240 to 350 nanometer range, such substrates need to be made of quartz because glass exhibits excessive ultraviolet light absorption in this region of the spectrum.

The referenced conductive coatings on the substrates must be sufficiently thin in order to comply with the transparency requirements outlined above. The minimum conductive coating film thickness allowable in such coatings is determined by the maximum allowable sheet resistance of the film which in turn is dependent on the pixel surface area. The mathematical relationship between these parameters is such that, for proper operation, the ratio between the pixel surface area and the film thickness must

equivalent of a pixel element. Since the typical pixel surface area to be used in mc applications of the present invention will be only 10 to 500 square microns, t conductive coating film thickness used for such applications can be adjusted to comp with the requirements for transparency to ultra violet light.

**Special procedures**

The two special procedures described in this section, a test procedure and : alternate interconnection procedure, are associated with the second, third and four embodiments of the present invention and are specifically recommended for very hi density micro arrays.

**The test and repair procedure** provides means for testing the integrity of eve transistor switch in the micro array. It consists of the sequence of steps which a outlined below with reference to the figures indicated in parenthesis:

(a) Defining on the polysilicon islands **210** (Fig. 12) the double polysilic transistor switches as described in the second embodiment of the prese invention;

(b) Defining the first layer metalization, comprising the following:
1. The gate control lines **114** (Fig. 12) within the micro array area;
2. The conductive trace extensions **139** (Fig. 2) of the gate control lines 1 (Fig. 10) within the peripheral metal interconnect system **138** (Fig. 1);
3. The conductive trace extensions **139** (Fig. 2) of the data lines **115** (F 10) within the peripheral metal interconnection system **138** (Fig. 1);
4. The gate area of the secondary control gates **127** (Fig. 10);

(c) Depositing and patterning a dielectric isolation layer covering entirely the g control lines **114** (Fig. 1) and the peripheral metal interconnect system 1 (Fig. 1). Such patterning must include contact openings to the seco metalization traces **142** (Fig. 2) in the peripheral metal interconnect syst **138** (Fig.1);

(d) Defining the second layer metalization, comprising the following:

1. Two interdigitated sets of temporary test lines placed over the areas corresponding to columns of pixels. The first set, comprises the temporary source test lines **132** (Fig. 12). Each of these test lines is connected to the source contacts **112** (Fig. 12) of all the transistor switches adjacent to the column of pixels over which that test line is placed. The second set, comprises the temporary drain test lines **133** (Fig. 12). Each of these test lines is connected to the primary drain contacts **126** (Fig. 12) of all the transistor switches adjacent to the column of pixels over which that test line is placed. In addition, these two sets of test lines will connect to the conductive trace extensions **139** (Fig. 1) of the data lines **115** (Fig. 10) defined during the first layer metalization as described in sections (b) 2. and (b) 3. above;
2. The second metalization of the peripheral metal interconnect system, comprising the intermetalization connections **140** (Fig. 14A), the second metalization traces **142** (Fig. 14A) and, if the intended configuration only comprises two metal layers, the circuit connecting pads **144** (Fig. 14A) which will be used as probing pads;

(e) This step, applicable only if the intended configuration comprises three metal layers, consists of depositing and patterning a dielectric isolation layer covering entirely the peripheral metal interconnect system **138** (Fig. 1) and including contact openings to the third metalization layer;

(f) This step, applicable only if the intended configuration comprises three metal layers, consists of defining the third layer metalization comprising the intermetalization connections **140** (Fig. 14B) and the circuit connecting pads **144** (Fig. 14B) which may incorporate the probing areas **344** (Fig. 14B);

(g) Testing every transistor switch in the micro array by probing the appropriate pads;

(h) Removing the primary gate connection to the gate control line **114** (Fig. 12) and primary drain connection to the drain test line **133** (Fig. 12) of an

transistor switches found to be defective and replacing the same by alternativ connections to the redundant counterparts of such defective transistor switche. This is done by means of the alternate interconnection procedure define below;

(i) Repeating the applicable portions of the above test procedure to verify that a replacement transistor switches are functional;

(j) Removing the temporary source test lines **132 (Fig. 12)**, the temporary drai test lines **133 (Fig. 12)**, the alternate gate connections **227 (Fig. 12)** and th alternate drain connections **228 (Fig. 12)**;

(k) Defining the pixel electrodes **104 (Fig. 10)** with the pixel tabs **116 (Fig. 1(** connected to the source contacts **112 (Fig. 10)** of the matching transistc switches;

(l) Depositing a layer of dielectric over the columns of pixel gaps **106 (Fig. 12** containing the transistor switches and patterning this dielectric, wher applicable due to failure of the primary transistor, with openings to the fir metal previously deposited over the gate area of the secondary control gate **127 (Fig. 12)**;

(m) Defining the secondary control gate connections **129 (Fig. 10)** wher applicable due to failure of the primary transistor switch;

(n) Depositing dielectric over the secondary control gate connections **129 (Fi 10)**;

(o) Defining the appropriate contact openings to the primary drain contact **12 (Fig. 10)** or to the secondary drain contact **128 (Fig. 10)**, as may b applicable.

(p) Defining data lines **115 (Fig. 10)** over the columns of pixel gaps **106 (Fi 10)** containing the transistor switches. These lines connect either the prima

drain contact 126 (Fig. 10) or the secondary drain contact 128 (Fig. 10), as may be applicable, of each transistor switch in that column of pixel gaps 106 (Fig. 10) to a matching conductive trace extension 139 (Fig. 1) in the peripheral interconnect system 138 (Fig. 1);

(q) Die attaching and testing the peripheral circuitry.

(r) Replacing peripheral circuits found to be defective.

(s) Connecting the peripheral circuits to the peripheral interconnect system.

The alternate interconnection procedure provides means for replacing every defective transistor switch in the micro array by an alternate transistor switch which is to operate in its place. It consists of the following sequence of steps applicable to each defective transistor switch:

(a) Locally removing by a selective photolithographic process the dielectric isolation and the metal over the defective gate area 225 (Fig. 12), which is the area where the gate control line 114 (Fig. 12) lies over the primary control gate 125 (Fig. 12) of the primary transistor switch;

(b) Locally removing by a selective photolithographic process the primary drain link 226 (Fig. 12) which is the connection between the drain test line 133 (Fig. 12) and the primary drain contact 126 (Fig. 12) of the defective transistor switch;

(c) Selectively depositing dielectric over the defective gate area 225 (Fig. 12) of the defective primary transistor switch;

(d) Defining appropriate contact openings to the gate control line, on both sides of the defective gate area 225 (Fig. 12);

(e) Defining the following alternate metal connections:

control line 114 (Fig. 12) to the secondary gate 127 (Fig. 12) of the defective transistor switch and bridges the gap generated on the gate control line 114 (Fig. 12) by step (a) above;

2. The alternate drain connection 228 (Fig. 12), which connects the temporary drain test line 133 (Fig. 12) to the secondary drain contact 128 (Fig. 12) of the defective transistor switch.

## OPERATION OF THE INVENTION

The operation of the programmable masking device which is the object of th present invention is described first with reference to Fig. 18 which illustrates the use o this device in direct imaging photolithographic applications. Next, the operation of th various embodiments of this device, is described with reference to Figs. 19, 20, 21 an 22 which illustrate the use of such embodiments in projection systems for visua display, three dimensional imaging, holographic imaging and printing systems respectively.

Fig. 18 is a pictorial representation of a photolithographic exposure apparatus illustrating the use of the programmable masking device, which is the object of the present invention, to generate images on a photosensitive target surface directly from data provided by a computer system, a technology presently described as direct imaging. This programmable masking device, built entirely of solid state elements, operates in conjunction with exposure systems in a manner similar to conventional non programmable masking devices. The apparatus of Fig. 18 comprises a light source 159 within a light housing 160 which is equipped with a light shutter 161. The light generated by the light source 159 is directed by the illumination optics 162 onto the surface of a programmable masking device 164 where it provides uniform illumination 163. A computer system 165 provides the pattern generation data necessary to generate the desired transparent images on the micro array of the programmable masking device 164. These images are then transferred by means of the exposure optics 166 onto the photosensitive target surface 167. Under normal operating conditions, the computer system 165 can download to the programmable masking device 164 the desired patterning data while the photosensitive target surface 167 is being aligned to the exposure optics. Upon completion of the alignment, the shutter 161 is momentarily opened for a preset exposure time. This cycle is then repeated with the next photosensitive target surface or the next site on the same photosensitive target surface.

In most photolithographic applications, typical exposure systems designed to operate with conventional masking devices, must be modified to accommodate the larger size of the programmable masking device which is the object of this invention. However, once installed, this programmable masking device needs only to be removed to perform repairs and maintenance or to install another programmable masking device

with different characteristics.

Other than installation, repair and maintenance, human intervention is not neede Under normal operating conditions, a computer system will be required for the use ( this programmable masking device. The computer system will fully support and contr such programmable masking device by downloading the required pattern generation da to the micro array memory. When appropriate, this computer will also provide contro to refresh and modify the patterns generated.

Some of the most significant photolithographic applications for thes programmable masking devices will be found in the semiconductor industry where suc devices will introduce manufacturing flexibility, improve yields, reduce cycle times an reduce manufacturing costs.

More specifically, these devices will provide means for repairing patternin defects on wafers, programming or altering the functionality of integrated circuits, co: effectively producing custom integrated circuits and generating complete systems on single wafer.

When the exposure apparatus is a wafer stepper, the computer system controllin the programmable masking device should be interfaced to such wafer stepper t synchronize the pattern generation with the mechanical stepping motion of the stepper.

Other very important applications of the present invention will be found in th cost effective manufacture of micro integrated systems comprising integrated circuits, i the die form, interconnected on a micro substrate. Such micro substrate will b produced by a technology similar to that used for the generation of the peripher interconnect system of the programmable masking devices which are the subject of th present invention.

The manufacture of the programmable masking devices provides another importar application for their use. As outlined in the section covering the description of th present invention, the fabrication of these programmable masking devices requires th use of programmable photolithography for performing repairs and making alterna

interconnections. Such programmable photolithography can be implemented with the use of another programmable masking device specifically configured for such application.

Fig. 19 illustrates the operation of the present invention in a visual display projection system. Such system comprises a light source 159 within a light housing 160. The light generated by the light source 159 is directed by the illumination optics 162 onto the surface of the programmable masking device 164 where it provides uniform illumination 163. A heat shield 168, is inserted in the light path to protect the programmable masking device 164 from the heat emitted by the light source 159. A video signal processing system 169 provides the digital video image generation data necessary to generate the desired transparent images on the micro array of the programmable masking device 164. These images are then transferred by means of the projection optics 170 onto a visual projection screen 171. Under normal operating conditions, the video signal processing system 169 continuously downloads to the programmable masking device 164 digital video imaging data at a rate compatible with video display imaging. The fifth embodiment of the present invention with the color imaging feature described previously would provide the proper features for the implementation of projection color television and multiple page computer monitor projection display systems.

Fig. 20 illustrates an application similar to that of Fig. 19 with the addition of a polarizer 172 for three dimensional projection viewing. All the elements described with reference to Fig. 19 have identical functions with reference to Fig. 20 and need not be repeated. The polarizer 172 is used in conjunction with polarizing glasses for three dimensional viewing. Under the control and synchronized by the video signal processing system 169, the polarizer 172 alternates the polarization of the light emerging from the programmable masking device 164 between two orthogonal planes, thus providing separate images for each one of the viewer's eyes.

Fig. 21 illustrates the use of this invention in holographic imaging applications. For such applications, a laser source 173 would emit a laser beam 174 which would be dispersed by the dispersion optics 175 to provide uniform laser illumination 176 over

holographic signal processing system 177 holographic patterns would be generated on the programmable masking device 164 which could be observed by the viewer 178. Since the patterns on the programmable masking device 164 could be continuously changed, the system described could provide means for the implementation of digitally controlled holographic television and computer monitor holographic viewing systems. Color holography could be implemented, as well, by the use of a laser source combining red, green and blue beams sequentially fired in synchronism with the viewing frames for each color generated by the holographic signal processing system 177.

Fig. 22 illustrates still another potential application for the present invention as a printing apparatus. It presumes that the imaging data is available in digital format such as that generated directly by a computer system or otherwise generated by digitizing a real image. Such apparatus would comprise a light source 159 within a light housing 160 equipped with a light shutter 161. The light generated by the light source 159 would be directed by the illumination optics 162 onto the surface of the programmable masking device 164 where it would provide uniform illumination 163. An image processing system 179 would provide the digitized imaging data necessary to generate the desired transparent images on the micro array of the programmable masking device 164. These images would then be transferred by means of the projection optics 170 an the operation of the light shutter 161 onto a photosensitive reproducing device 180. This photosensitive reproducing device 180 would subsequently produce hard copies of the images defined on its surface. For simplicity, Fig. 22 depicts the photosensitive reproducing device 180 in a planar configuration. However, a cylindrical configuration such as the conventional drum of most modern office printing machines could also be used provided the projection optics would be equipped with a scanning device synchronized with the movement of such drum.

## CONCLUSIONS, RAMIFICATIONS AND SCOPE

Accordingly, the electronically programmable masking device, which is the subject of the present invention, introduces a new level of flexibility in the industrial use of photolithography by providing the capability for translating computer aided design (CAD) data, directly into images produced on a photosensitive target surface. At the

same time, it opens new opportunities in the fields of high definition projection color television, multiple page computer monitor projection display systems, holographic television, holographic computer monitor systems and printing devices. Some of the most important applications of the present invention will be found in the semiconductor industry, which is highly dependent upon the use of microlithography. The technology provided by the present invention will open the door to major evolutions in this industry in that:

* it will permit the design and manufacture of small volume custom integrated circuits to be done at a cost comparable to that of commercial integrated circuits produced in high volume;

* it will permit the cost effective development of wafer scale integration, a technology whereby complete electronic systems, such as computers, can be built on a single wafer;

* it will provide the means to substantially increase semiconductor manufacturing yields by offering a technology for pattern repair; and

* it will provide means to substantially reduce product development and manufacturing cycle times.

While the descriptions herein contain many specificities, these should not be construed as limiting the scope of the present invention but as merely providing illustrations of some of the most relevant embodiments of the present invention.

For example, this electronically programmable masking device could be used in the printed circuit board industry to perform direct imaging from printed circuit layout data provided by computer systems.

Accordingly, the scope of the present invention should be determined not by the embodiments illustrated, but by the appended claims and their legal equivalents.

## CLAIMS

1. In an imaging system including a source of illumination, illumination optics, a masking device, and projection optics for directing light passing through said masking device onto a target surface, an improved masking device comprising:

means forming a liquid crystal micro array including a plurality of contiguous discreet programmable pixels wherein each of said pixels functions as a light valve for the light directed onto said target surface; and

means responsive to externally generated input control signals for individually controlling in real time the optical light valve state of each of said pixels.

2. An improved masking device as recited in claim 1 wherein the size of the image of each of said programmable pixels on the target surface is equal to or is a sub multiple of the minimum feature size to be generated on the target surface.

3. An improved masking device as recited in claim 2 wherein adjacent pixels are separated by gaps of predetermined width and wherein the width of the gap between any two adjacent pixels is less than the minimum size which can be resolved by said optics so that patterns imaged on a target surface are free of gaps between adjacent pixels.

4. An improved masking device as recited in claim 1 wherein said liquid crystal micro array is comprised of:

a transparent primary substrate coated on one side with a transparent conductive film patterned to form an array of pixel electrodes and coated on a second side with a light-polarizing film;

a transparent secondary substrate coated on one side with a continuous transparent conductive film forming a common electrode for said array of said pixel electrodes and coated on a second side with a light-polarizing film;

means for precisely spacing and aligning said primary and said secondary substrates parallel to each other so that said one sides form the opposite sides of a flat sealed chamber;

a liquid crystal material disposed within said chamber;

an array of transistor switches formed on the surface of said primary substrate and

configured such that each of said switches is associated with one of said pixel electrodes;

a set of electronic control lines formed by conductive material deposited on the surface of said primary substrate;

a set of electronic data lines formed by conductive material deposited on the surface of said primary substrate;

means for interconnecting the control electrode of each of said transistor switches to one of said control lines;

means for interconnecting each of said pixel electrodes to one of said data lines via an electronically switchable connection made by one of said transistor switches; and

means for coupling said input control signals to said control lines and said data lines.

5. An improved masking device as recited in claim 4 wherein for the purpose of reducing the effective sheet resistivity of said common electrode, said secondary substrate further includes an opaque conductive film patterned over those areas of said secondary substrate delineated by the shadow of the space not occupied by the pixel electrodes on said primary substrate when said programmable masking device is operated under intended illumination conditions.

6. An improved masking device as recited in claim 5 wherein for the purposes of providing a precise optical definition of the edges of each of said pixels in said micro array, the transparent area of each of said pixels is optically defined by the edges of said opaque conductive film formed on said secondary substrate.

7. An improved masking device as recited in claim 6 and further including a discreet color filter optically associated with each said pixel, the color of each said color filter being selected from the group consisting of red, green and blue colors, said color filters being respectively positioned relative to adjacent color filters such that a particular grouping of said color filters define a pattern which is repeated over said micro array of programmable pixels.

8. An improved masking device as recited in claim 4 wherein said array of transistor [illegible] associated with each of said

pixel electrodes, and at least one secondary transistor switch associated with each of said pixel electrodes as means of providing transistor switch redundancy, and further including means for substituting through alternative interconnections, one of said secondary transistor switches for one of said primary transistor switches.

9. An improved masking device as recited in claim 4 wherein for each interconnection formed via said control lines and said data lines at least one alternate interconnection is provided.

10. An improved masking device as recited in claim 9 wherein said alternative interconnections are created by forming said control lines and said data lines with multiple layers of conductive material directly superimposed upon each other with each layer being generated with a separate photolithographic operation as a means of statistically insuring that defects on one layer do not coincide with defects on another layer, in turn statistically insuring that said control lines and said data lines are free of undesirable discontinuities.

11. An improved masking device as recited in claim 9 wherein said alternative interconnections are created by locally deposited a bridging metal trace over any discontinuity identified in said control lines and said data lines.

12. An improved masking device as recited in claim 4 wherein said primary substrate is extended to include an area laying outside the periphery of said micro array;

a set of drive integrated circuits disposed upon said area and providing means for controlling the optical light valve state of each of said pixels;

a set of interface integrated circuits disposed upon said area and providing means for interfacing and data linking said drive integrated circuits to an external computer system for electronically processing and generating the desired patterning data;

a multi-layer metalization system formed upon said substrate within said area;

a set of bonding pads formed upon said substrate within said area providing means for connecting said set of drive integrated circuits and said set of interface integrated circuits to said multiple layer metalization system;

means for connecting said set of control lines and said set of data lines to appropriate points on said multiple layer metalization system.

a set of probing pads formed upon said substrate within said area providing means for connecting external test systems to appropriate test points of said multiple layer metalization system, said test points being such as to provide means for testing the integrity of the electronic system of said programmable masking device; and

means for connecting said set of interface circuits to a data communications connector system incorporated in said primary substrate wherein said data communications connector system can provide an interconnection to an external data communications link providing access to said external computer system.

13. An improved masking device as recited in claim 12 wherein said data communications connector system includes a coupling device for each data communications line and wherein the physical components of the transmitter portion and the receiver portion of said coupling device are physically isolated from each other so as to insure that no mechanical strain is applied to said programmable masking device by said connector system.

14. An improved masking device as recited in claim 13 wherein said transmitter portion is an infrared transmitting device and said receiver portion is an infrared receiving device.

15. An improved masking device as recited in claim 4 wherein said means for controlling the light valve state of each of said pixels includes means for controlling the voltage applied between each of said pixel electrodes and said common electrode thereby providing means for modulating the transparency of each of said pixels.

16. An improved masking device as recited in claim 15 wherein said means for controlling the voltage applied between each of said pixel electrodes and said common electrode includes a digital-to-analog converter circuit.

17. An improved masking device as recited in claim 1 wherein the optical characteristics of each said light valve are compatible with their use in conjunction with photolithographic exposure systems operating with ultraviolet illumination in the range of 240 to 470 nanometers.

18. A method for testing the integrity of the transistor switches of a programmable masking device including a micro array of discrete pixel electrodes disposed in an orderly array of rows and columns on a transparent substrate forming one wall of a chamber containing a liquid crystal material, a first set of electrical conductors disposed to overlay rows of spaces separating adjacent rows of said electrodes, a second set of electrical conductors disposed to overlay columns of spaces between said electrodes directed orthogonal to said rows of spaces and an array of transistor switches, each of which is disposed proximate on the intersection of ones of said first and second conductors and electrically connected thereto for selectively applying a controlled voltage to a selected pixel electrode, comprising the steps of

defining by means of photolithographic processes a set of electrical interconnections linking each of the electrodes of each of said transistor switches in said array to a set of probing pads on the periphery of said micro array, said set of probing pads providing means for electrically accessing each of said transistor switches;

performing predetermined electrical tests to establish the integrity of each of said transistor switches; and

removing by means of photolithographic processes the portions of said electrical interconnections which have no further use in the final configuration of said programmable masking device.

19. A method for substituting the interconnections of any primary transistor switch of a programmable masking device which may be defective by making interconnection to a matching secondary transistor switch in a micro array of discrete pixel electrodes disposed in an orderly array of rows and columns on a transparent substrate forming one wall of a chamber containing a liquid crystal material, a first set of electrical conductors disposed to overlay rows of spaces separating adjacent rows of said electrodes, a second set of electrical conductors disposed to overlay columns of spaces between said electrodes directed orthogonal to said rows of spaces and an array of transistor switches, each including a primary transistor device and a secondary transistor device disposed proximate on the intersection of ones of said first and second conductors and electrically connected thereto for selectively applying a controlled voltage to a selected pixel electrode, comprising the steps of:

removing by means of selective photolithographic processes the portions of the electrical interconnections linking the primary gate and the primary drain of each said

primary transistor switch which has no further use in the final configuration of said programmable masking device; and

defining and generating by means of selective photo-lithographic processes an alternative set of inter-connections to each said secondary transistor switch which will be required to operate in place of a corresponding primary transistor switch found to be defective.

20. A method of direct imaging onto a target surface patterns defined by patterning data provided by a computer system, comprising the steps of:

providing a source of illumination;

providing a programmable masking device including a liquid crystal micro array having a plurality of contiguous discrete programmable pixels responsive to electrical inputs and each of which pixels functions as a light valve for blocking or transmitting light;

providing means for directing light from said light source through said masking device and onto said target surface; and

providing electronic means for selectively programming each of said programmable pixels so that light passing through said masking device forms a desired image on said target surface.

21. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and is a patterned substrate and wherein the image cast onto said substrate is used to photolithographically repair patterning defects previously identified on said patterned substrate.

22. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and the light passing through said masking device is used to alter the functionality of a solid state circuit formed upon said target surface by altering specific patterns on said solid state circuits in response to digital data generated by said computer system and input to said masking device to control the pattern of light generated thereby.

23. A method of direct imaging onto a target surface as recited in claim 20 wherein

said target surface to have specific patterns altered thereon in response to electronic signals input to said masking device by said computer system.

24. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and further comprising the step of employing said image to produce custom solid state circuits by generating the specific patterns required for production thereof directly from digital data provided by said computer system.

25. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and further comprising the step of employing said image to change from site to site the patterns printed on a substrate with the use of a step-and-repeat exposure system.

26. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and further including the step of employing said image to produce electronic inter-connections in electronic devices disposed on said photo-sensitive target surface.

27. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is a visual projection screen and wherein each pixel of the projected image corresponds to digitized video information input to said masking device from a computing system.

28. A method of direct imaging onto a target surface as recited in claim 20 wherein said programmable pixels are formed by pixel electrodes and a common electrode having a liquid crystal material disposed therebetween and further comprising the step of:

controlling the voltage applied between said pixel electrodes and said common electrode to control the light valve state of each of said pixels thereby providing means for modulating the transparency of each of said pixels.

29. A method of direct imaging onto a target surface as recited in claim 28 and further comprising the step of:

providing a digital-to-analog converter circuit for controlling the voltage applie

between each of said pixel electrodes and said common electrode.

30. A method of direct imaging onto a target surface as recited in claim 20 for generating in real time three-dimensional digitized video images by causing said programmable masking device to alternatively develop cross-polarized images which when viewed with polarizing eyeglasses appear to a viewer to provide a three-dimensional image.

31. A method of direct imaging onto a target surface as recited in claim 20 and further comprising using said masking device to generate, in real time, holographic images in response to digitized holographic video data input thereto from a computing means.

32. A method of direct imaging onto a target surface as recited in claim 20 wherein said target surface is photosensitive and further comprising projecting the image cast by said masking device into a printing means to reproduce on paper digitized video images corresponding to digitized video signals input to said masking device from a computing means.

33. A method of providing a masking device for use in conjunction with a source of illumination, illumination optics, and exposure optics for directing light through said masking device and onto a target surface, comprising the steps of:

providing a transparent primary surface coated on one side with a transparent conductive film patterned to form an array of pixel electrodes and coated on a second side with a light-polarizing film;

providing a transparent secondary substrate coated on one side with a continuous transparent conductive film forming a common electrode for said array of pixel electrodes and coated on a second side with a light-polarizing film;

providing means for precisely spacing and aligning said primary and said secondary substrates parallel to each other so that said one sides form the opposite sides of a flat sealed chamber;

providing a liquid crystal material disposed within said chamber;

forming an array of transistor switches on the surface of said primary substrate

electrodes;

forming a set of control lines by depositing conductive material on the surface of said primary substrate;

forming a set of data lines by depositing conductive material on the surface of said primary substrate;

providing means for interconnecting the control electrode of each of said transistor switches to one of said control lines;

providing means for interconnecting each of said pixel electrodes to one of said data lines via an electrically switchable connection made by one of said transistor switches; and

providing a means for coupling input control signals to said control lines and said data lines.

34. A method of providing a masking device as recited in claim 33 and further comprising the step of:

reducing the effective sheet resistivity of said common electrode by providing an opaque conductive film on said secondary substrate over those areas of said second substrate delineated by the shadow of the spaces separating the pixel electrodes on said primary substrate when said programmable masking device is operated under intended illumination conditions.

35. A method of providing a masking device as recited in claim 34 and further comprising the step of:

optically defining the edges of said opaque conductive film formed on said secondary substrate to provide a precise optical definition of the edges of each of said pixels in said micro array.

36. A method of providing a masking device as recited in claim 33 and further comprising the step of:

providing a discrete color filter in optical association with each said pixel electrode, the color of each said color filter being selected from the group consisting of red, green and blue colors, said color filters being respectively positioned relative to adjacent color filters such that a particular grouping of said color filters defines a

37. A method of providing a masking device as recited in claim 33 and further comprising the steps of:

configuring said array of transistor switches to have one primary transistor switch and at least one secondary transistor switch associated with each of said pixel electrodes to provide transistor switch redundancy; and

providing means for substituting, through alternative interconnections, one of said secondary transistor switches for one of said primary transistor switches.

38. A method of providing a masking device as recited in claim 33 and further comprising the step of:

forming at least one alternative interconnection for each interconnection formed via said control lines and said data lines.

39. A method of providing a masking device as recited in claim 38 and further comprising the step of:

creating said alternative interconnections by forming said control lines and said data lines with multiple layers of conductive material directly superimposed upon each other with each layer being generated by a separate photo-lithographic operation as a means of statistically insuring that defects on one layer do not coincide with defects on another layer so as to statistically insure that said control lines and said data lines are free of undesirable discontinuities.

40. A method of providing a masking device as recited in claim 33 and further comprising the step of:

repairing discontinuities in said data lines and said control lines by locally depositing a bridging metal trace over any discontinuity identified therein.

41. A method of providing a masking device as recited in claim 33 and further comprising the steps of:

extending said primary substrate to include an area on the periphery of said micro array forming a multilayer metalization system in said area;

disposing a set of integrated driver circuits upon said area to provide means for

disposing a set of integrated interface circuits upon said area to provide means for interfacing and data-linking said integrated driver circuits to an external computer system for electronically processing and generating desired patterning data;

forming a set of bonding pads to provide means for connecting said set of integrated driver circuits and said set of integrated interface circuits to said multiple layer metalization system;

providing means for connecting said set of control lines and said set of data lines to appropriate points on said multiple layer metalization system;

providing a set of probing pads in said area to connect external test systems to appropriate test points of said multiple layer metalization system, said test points being such as to provide means for testing the electrical integrity of said programmable masking device; and

providing means for connecting said set of interface circuits to a data communications connector system incorporated in one of said substrates to provide an inter-connection to an external data communication link providing access to an external computer system.

42. A method of providing a masking device as recited in claim 41 and further comprising the step of:

providing a coupling device for each data communications line in said connector system and for causing the physical components of the transmitting portion and the receiving portion of said coupling device to be physically isolated from each other so as to insure that no mechanical strain is applied to said programmable masking device by said connector system.

43. A method of providing a masking device as recited in claim 42 and further comprising the step of:

providing an infrared transmitting device for use in said transmitting portion and providing an infrared receiving device for use in said receiving portion.

44. A method of providing a masking device as recited in claim 33 and further comprising the step of:

controlling the voltage applied between said pixel electrodes and said common

for modulating the transparency of each of said pixels.

45. A method of providing a masking device as recited in claim 44 and further comprising the step of:

providing a digital-to-analog converter circuit for controlling the voltage applied between each of said pixel electrodes and said common electrode.

46. A method of providing a masking device as recited in claim 33 and further comprising the step of:

selecting the optical characteristics of each said light valve to be compatible with its use in conjunction with exposure systems operating with ultraviolet illumination in the range of 240-470 nanometers.

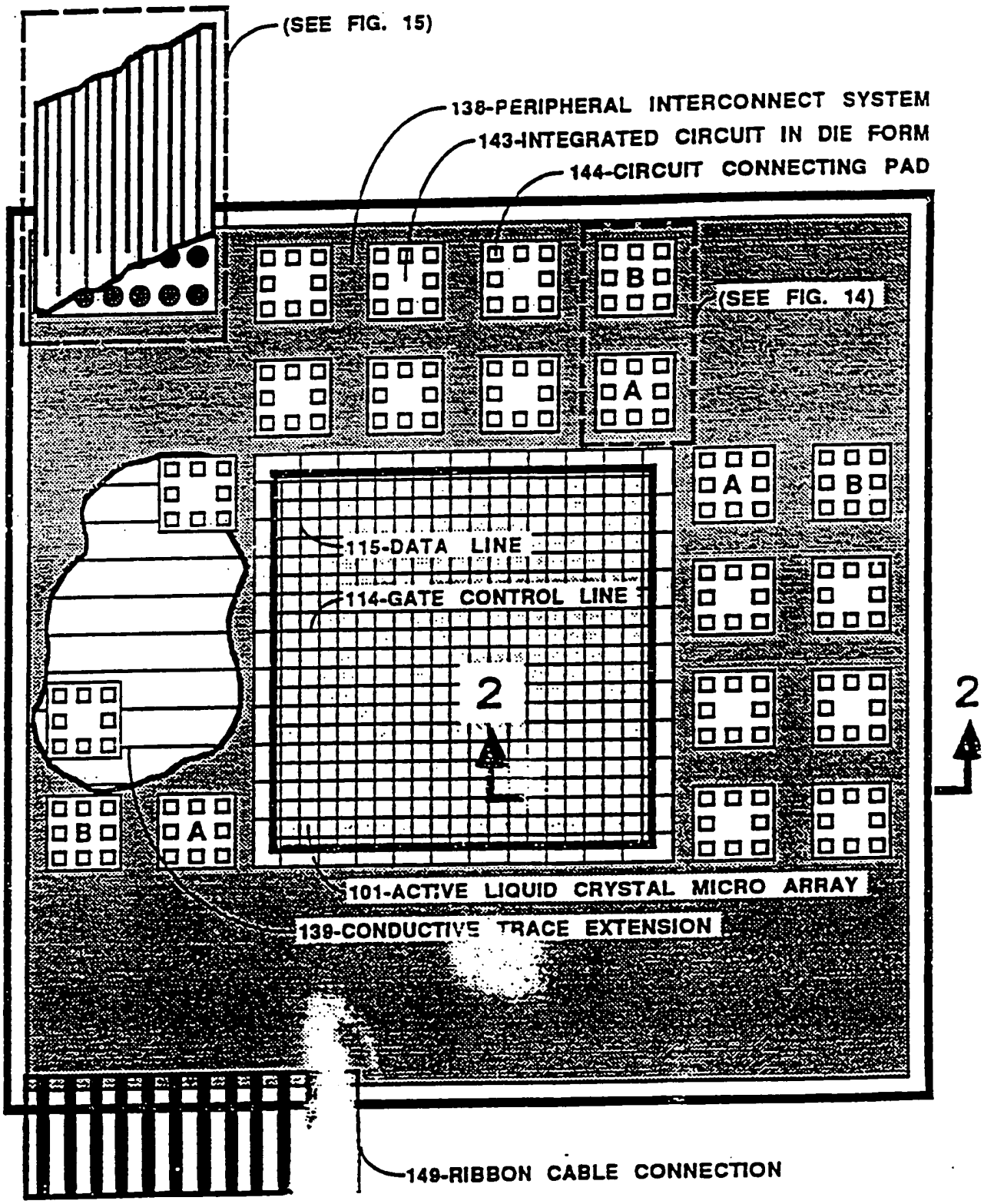

(SEE FIG. 15)
138-PERIPHERAL INTERCONNECT SYSTEM
143-INTEGRATED CIRCUIT IN DIE FORM
144-CIRCUIT CONNECTING PAD
(SEE FIG. 14)
115-DATA LINE
114-GATE CONTROL LINE
2
2
101-ACTIVE LIQUID CRYSTAL MICRO ARRAY
139-CONDUCTIVE TRACE EXTENSION
149-RIBBON CABLE CONNECTION

Fig. 1

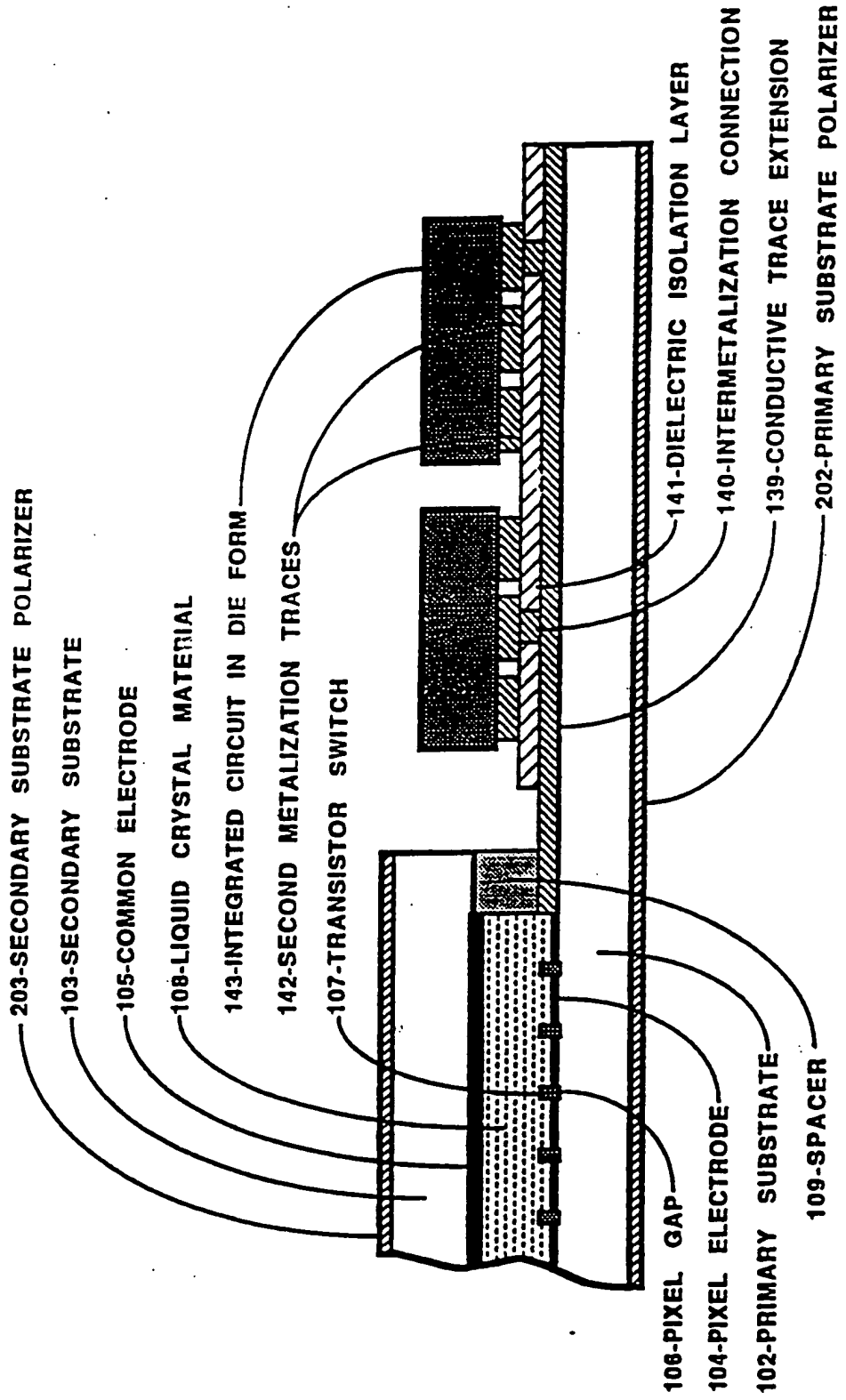

203-SECONDARY SUBSTRATE POLARIZER
103-SECONDARY SUBSTRATE
105-COMMON ELECTRODE
108-LIQUID CRYSTAL MATERIAL
143-INTEGRATED CIRCUIT IN DIE FORM
142-SECOND METALIZATION TRACES
107-TRANSISTOR SWITCH
141-DIELECTRIC ISOLATION LAYER
140-INTERMETALIZATION CONNECTION
139-CONDUCTIVE TRACE EXTENSION
202-PRIMARY SUBSTRATE POLARIZER
106-PIXEL GAP
104-PIXEL ELECTRODE
102-PRIMARY SUBSTRATE
109-SPACER

Fig. 2

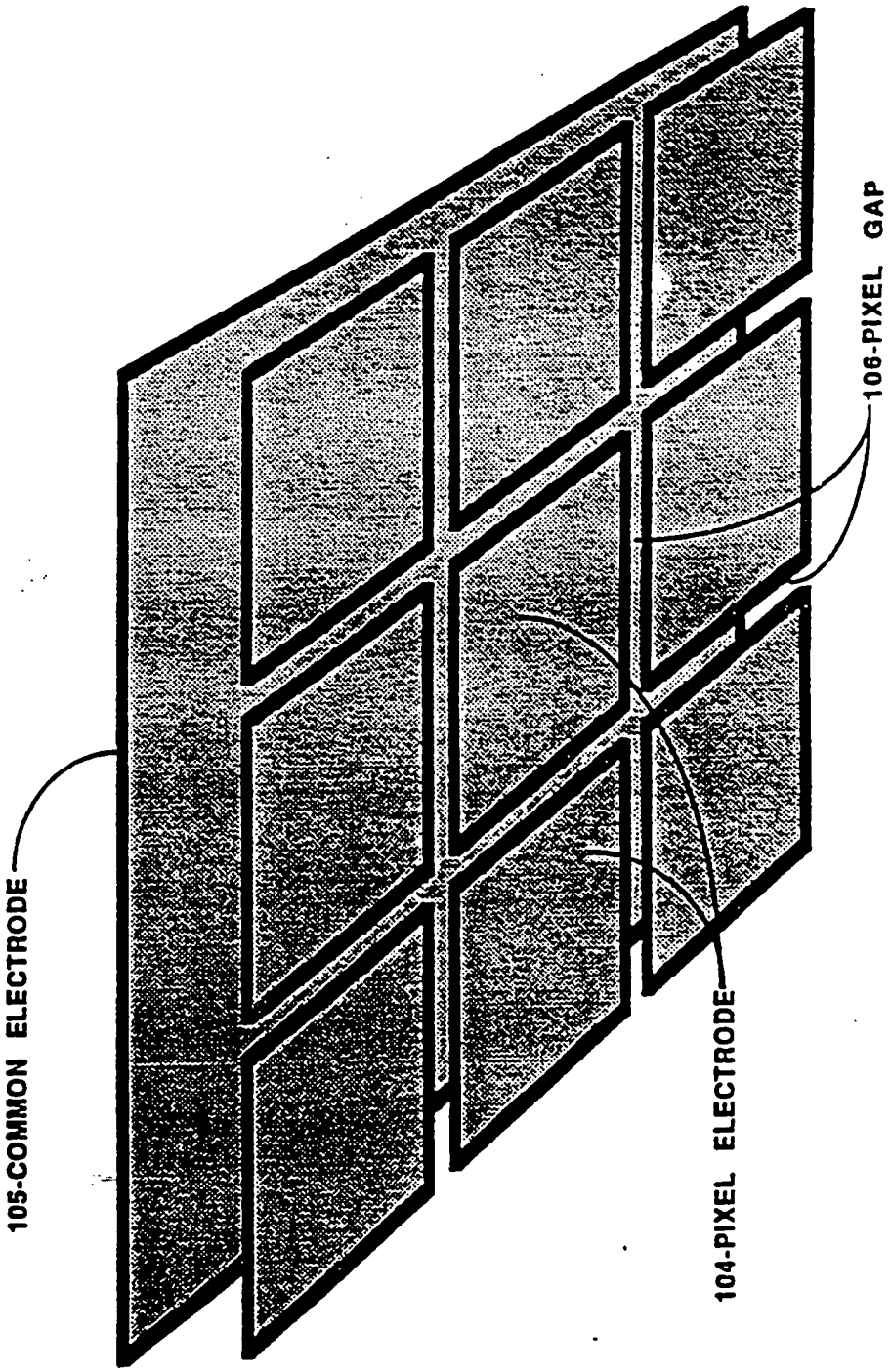



Fig. 3

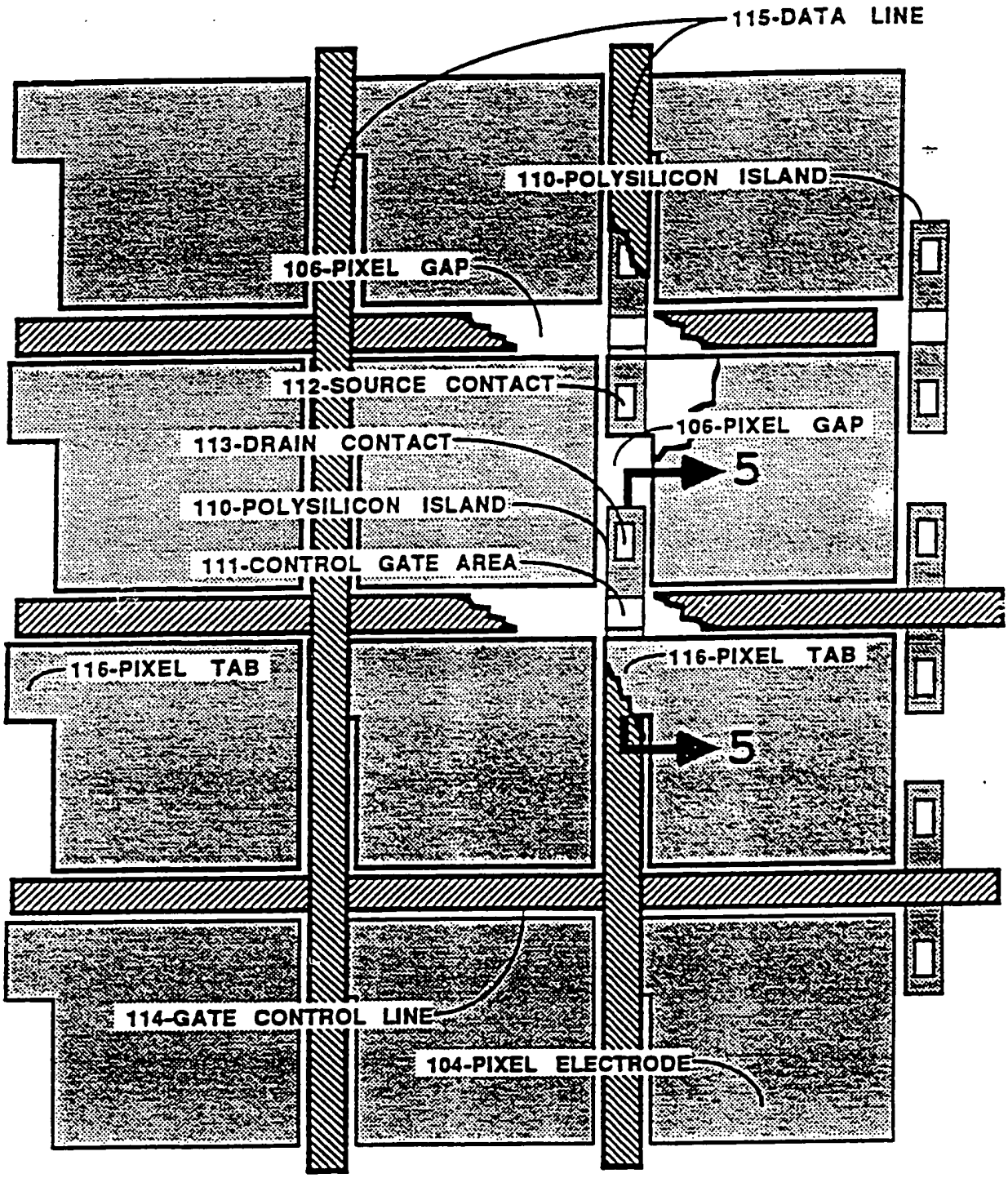

115-DATA LINE
110-POLYSILICON ISLAND
106-PIXEL GAP
112-SOURCE CONTACT
106-PIXEL GAP
113-DRAIN CONTACT
5
110-POLYSILICON ISLAND
111-CONTROL GATE AREA
116-PIXEL TAB
116-PIXEL TAB
5
114-GATE CONTROL LINE
104-PIXEL ELECTRODE

Fig. 4

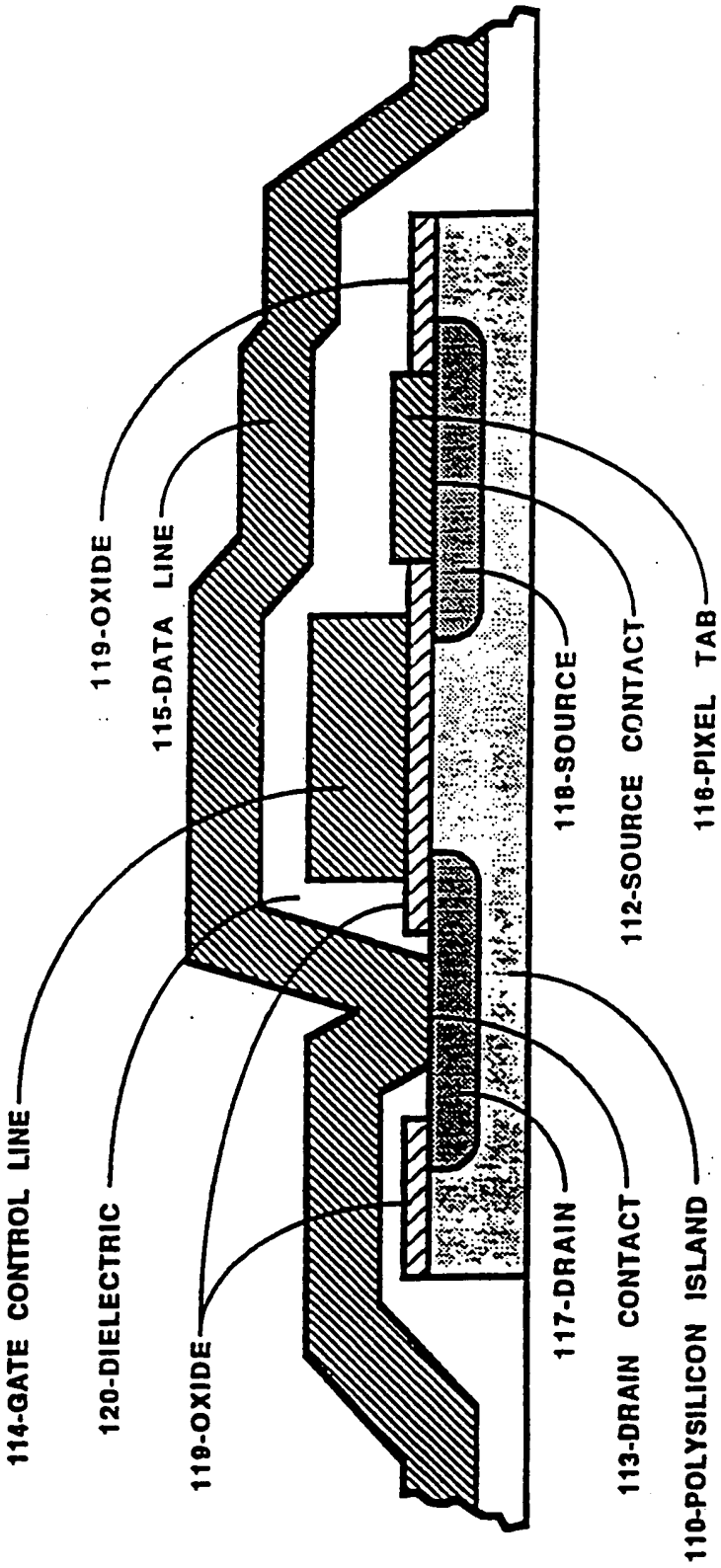

114-GATE CONTROL LINE
120-DIELECTRIC
119-OXIDE
119-OXIDE
115-DATA LINE
118-SOURCE
112-SOURCE CONTACT
116-PIXEL TAB
117-DRAIN
113-DRAIN CONTACT
110-POLYSILICON ISLAND

Fig. 5

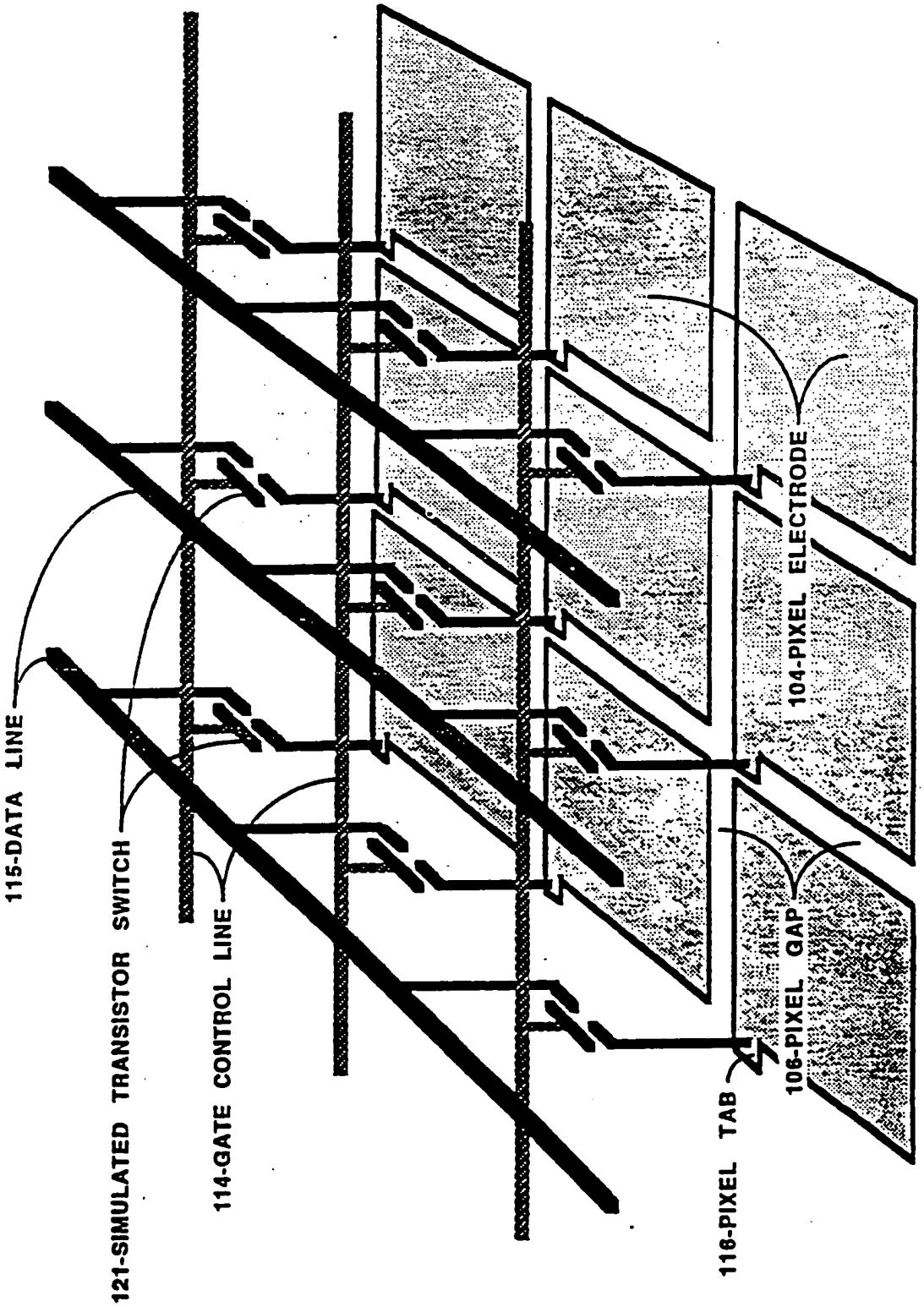

115-DATA LINE
121-SIMULATED TRANSISTOR SWITCH
114-GATE CONTROL LINE
116-PIXEL TAB
108-PIXEL GAP
104-PIXEL ELECTRODE

Fig. 6

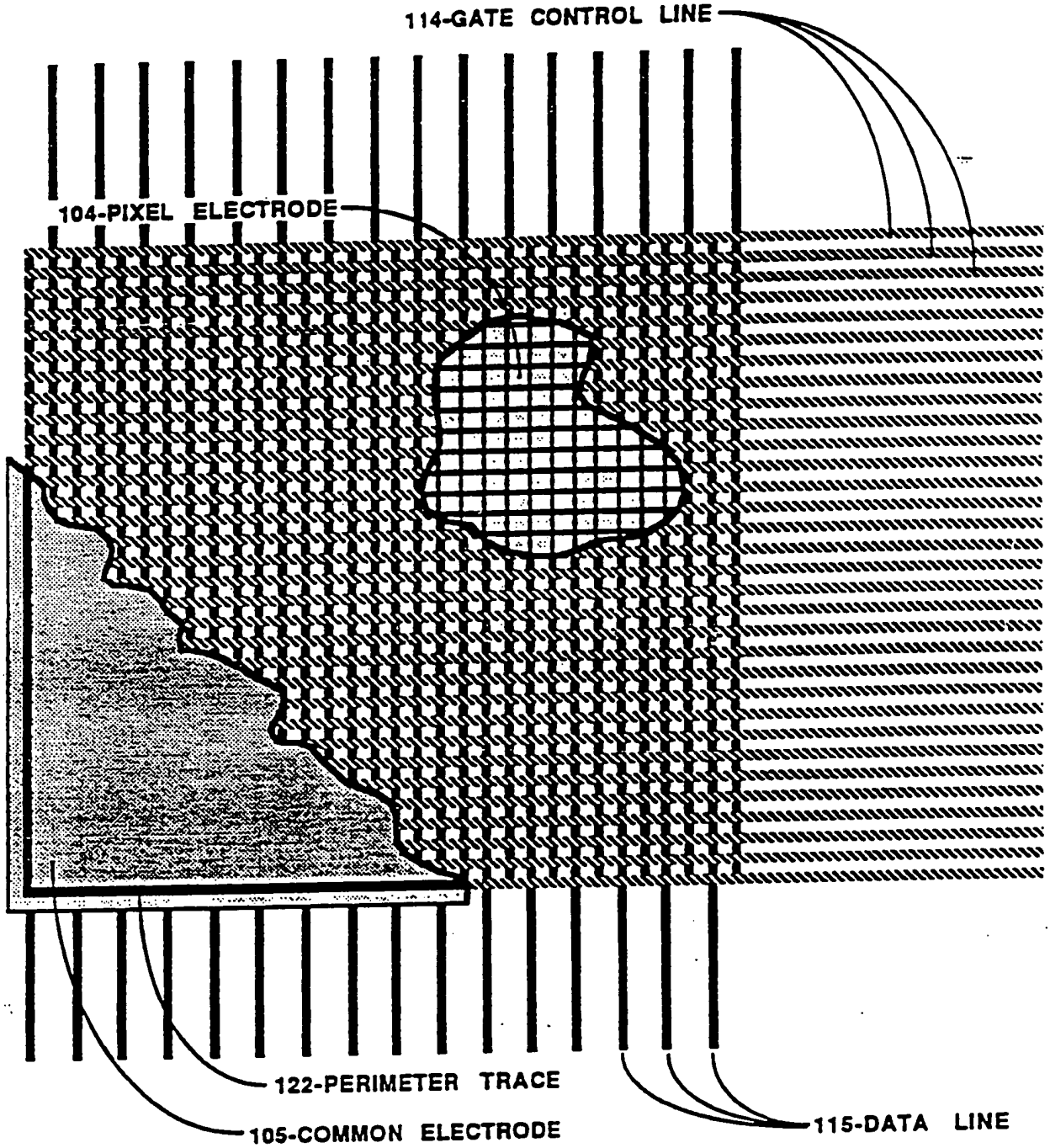

114-GATE CONTROL LINE
104-PIXEL ELECTRODE
122-PERIMETER TRACE
105-COMMON ELECTRODE
115-DATA LINE

Fig. 7

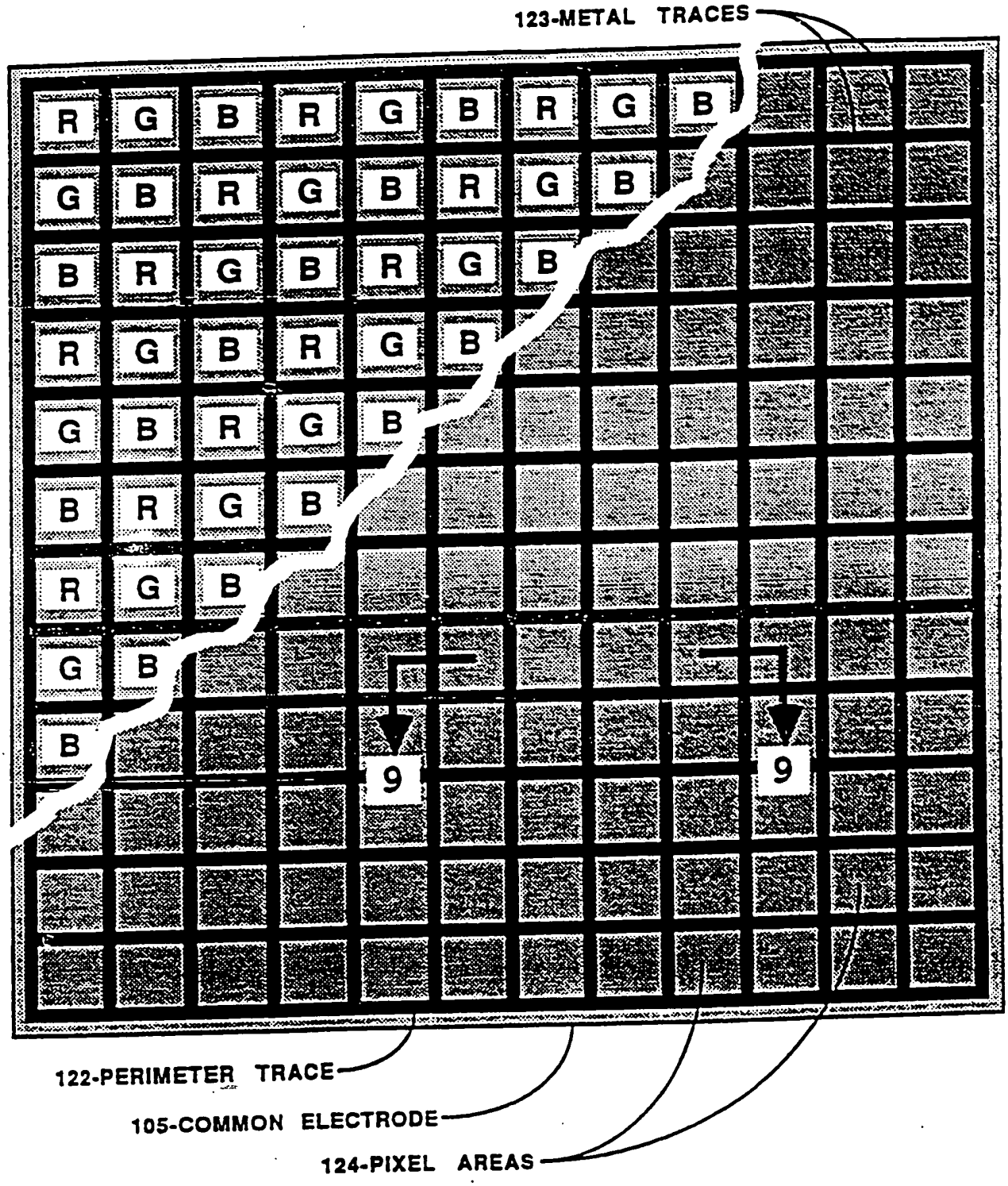

123-METAL TRACES
R G B R G B R G B
G B R G B R G B
B R G B R G B
R G B R G B
G B R G B
B R G B
R G B
G B
B
9
9
122-PERIMETER TRACE
105-COMMON ELECTRODE
124-PIXEL AREAS

Fig. 8

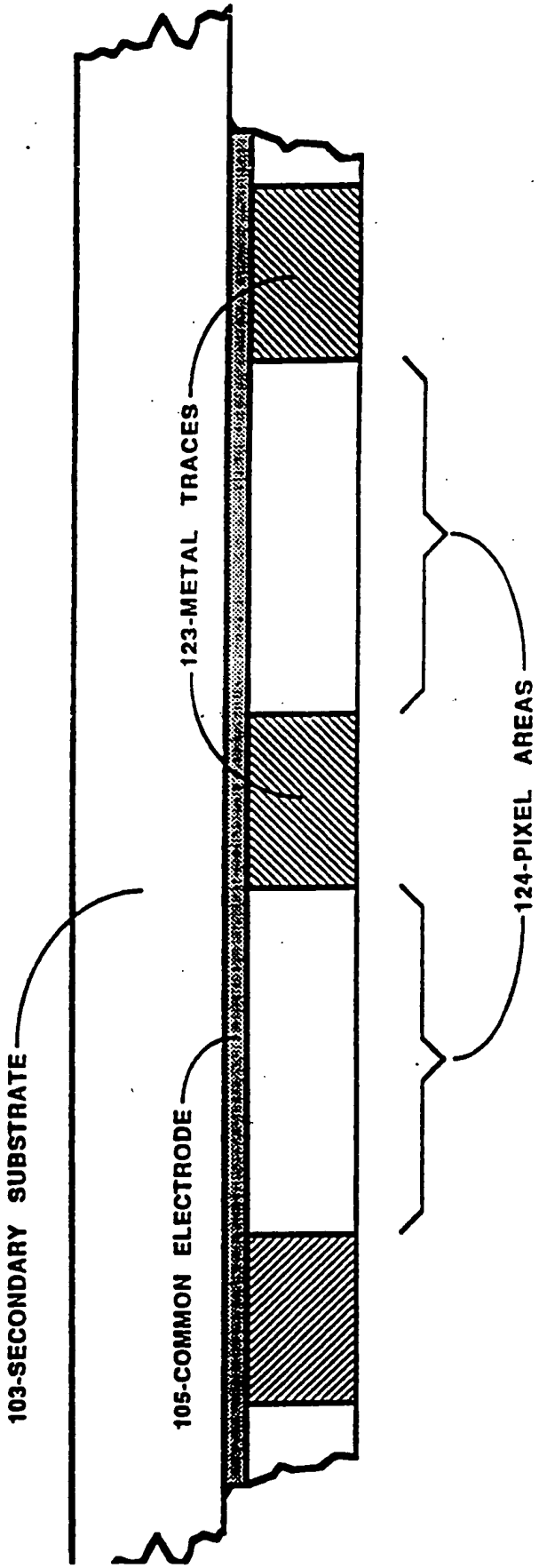

103-SECONDARY SUBSTRATE
105-COMMON ELECTRODE
123-METAL TRACES
124-PIXEL AREAS

Fig. 9

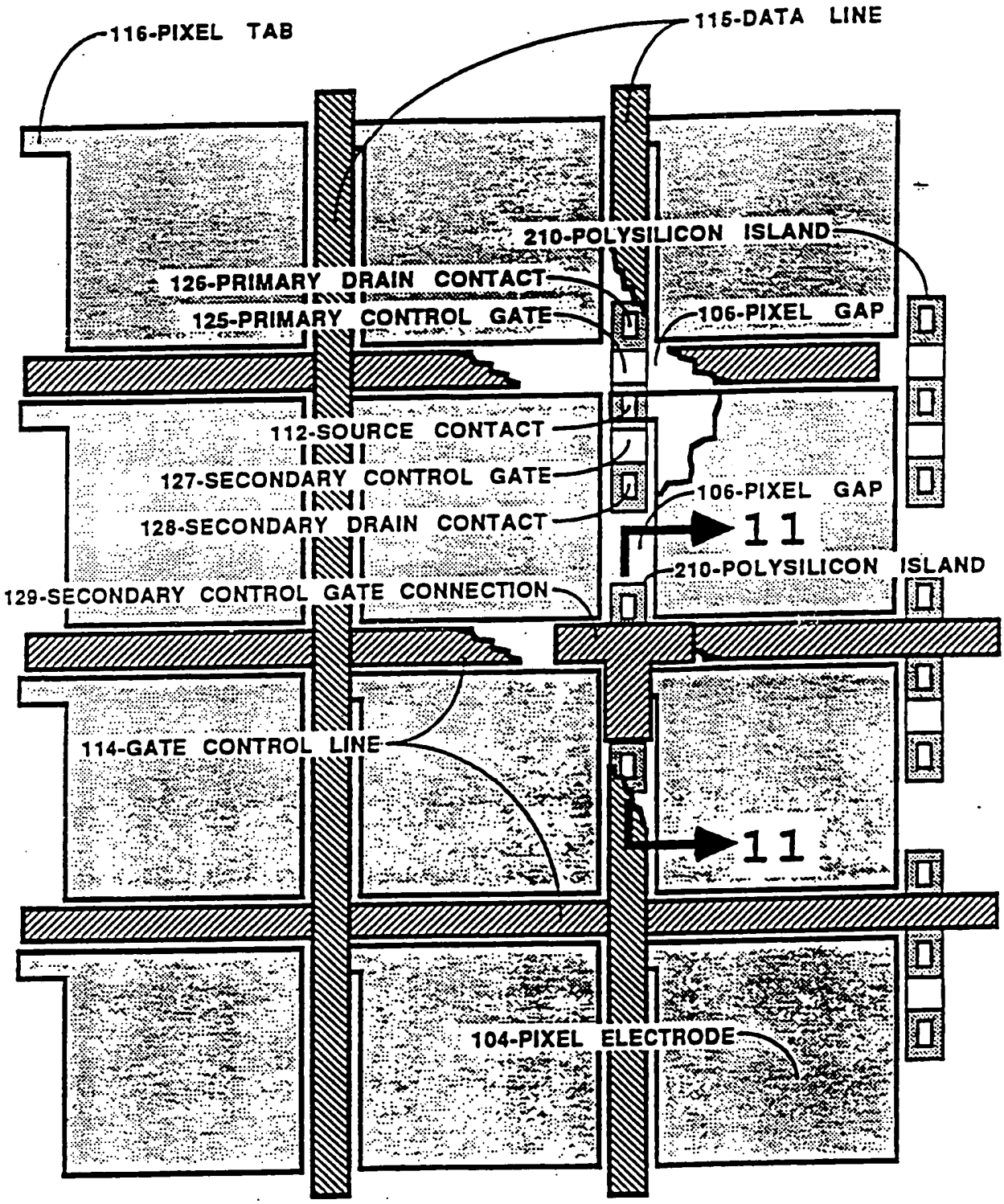

116-PIXEL TAB
115-DATA LINE
210-POLYSILICON ISLAND
126-PRIMARY DRAIN CONTACT
125-PRIMARY CONTROL GATE
106-PIXEL GAP
112-SOURCE CONTACT
127-SECONDARY CONTROL GATE
106-PIXEL GAP
128-SECONDARY DRAIN CONTACT
11
210-POLYSILICON ISLAND
129-SECONDARY CONTROL GATE CONNECTION
114-GATE CONTROL LINE
11
104-PIXEL ELECTRODE

Fig. 10

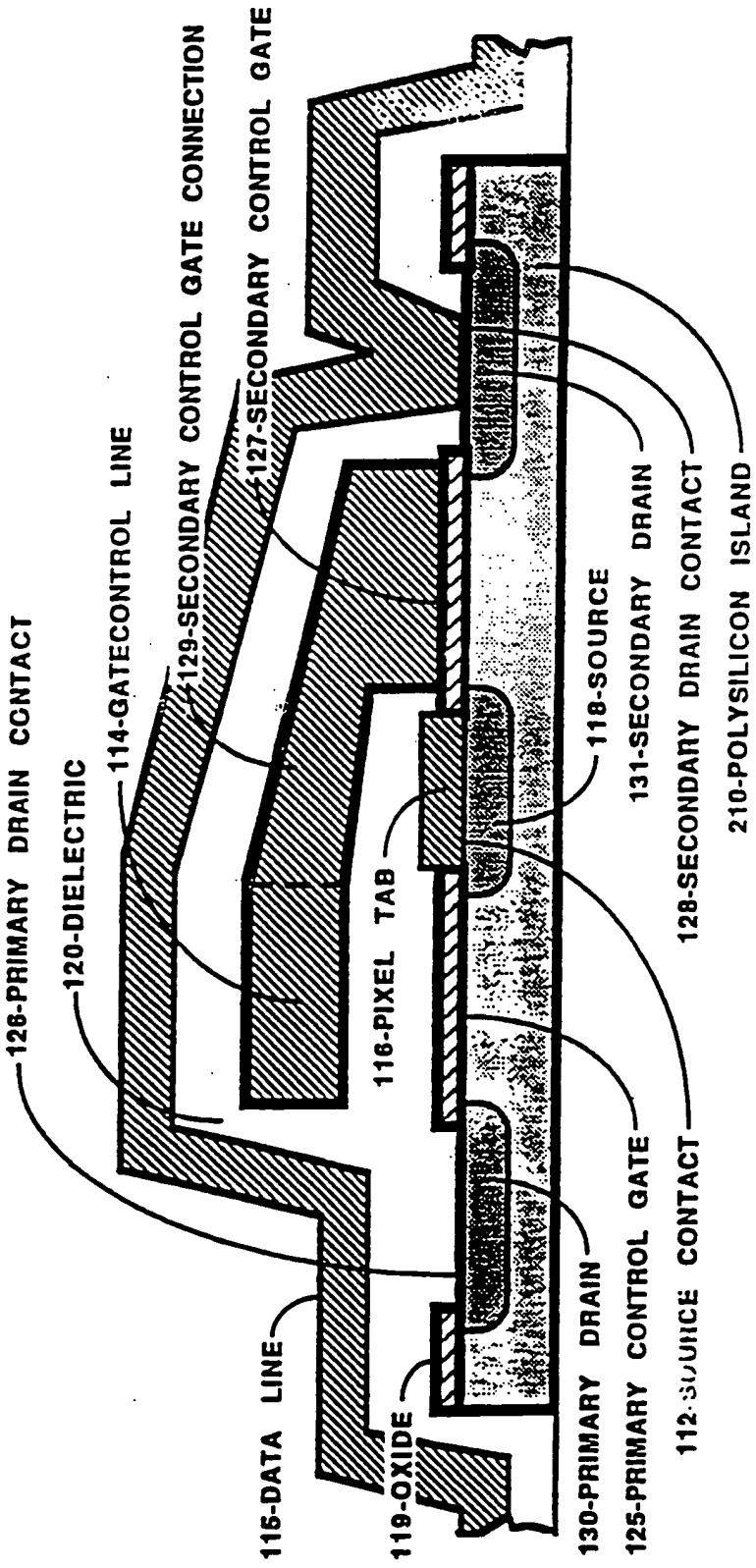

126-PRIMARY DRAIN CONTACT
120-DIELECTRIC
114-GATECONTROL LINE
129-SECONDARY CONTROL GATE CONNECTION
127-SECONDARY CONTROL GATE
116-PIXEL TAB
118-SOURCE
131-SECONDARY DRAIN
128-SECONDARY DRAIN CONTACT
210-POLYSILICON ISLAND
115-DATA LINE
119-OXIDE
130-PRIMARY DRAIN
125-PRIMARY CONTROL GATE
112-SOURCE CONTACT

Fig. 11

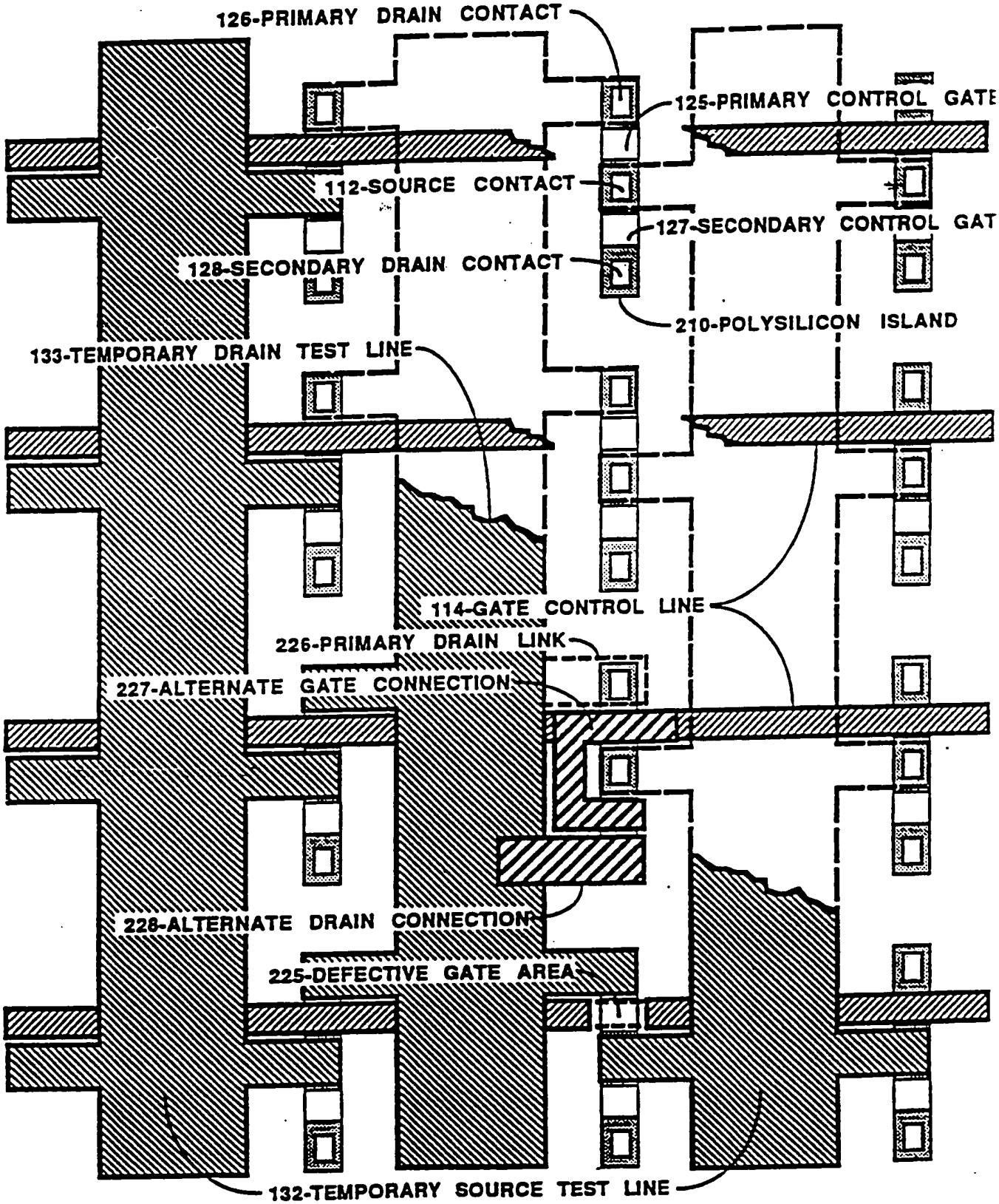

126-PRIMARY DRAIN CONTACT
125-PRIMARY CONTROL GATE
112-SOURCE CONTACT
127-SECONDARY CONTROL GAT
128-SECONDARY DRAIN CONTACT
210-POLYSILICON ISLAND
133-TEMPORARY DRAIN TEST LINE
114-GATE CONTROL LINE
226-PRIMARY DRAIN LINK
227-ALTERNATE GATE CONNECTION
228-ALTERNATE DRAIN CONNECTION
225-DEFECTIVE GATE AREA
132-TEMPORARY SOURCE TEST LINE

Fig. 12

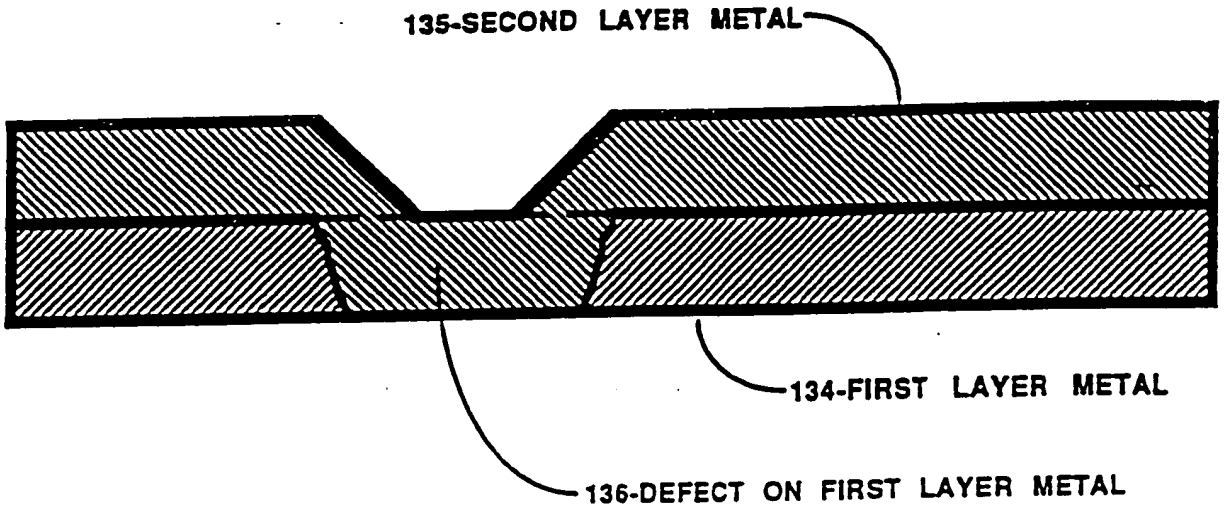



Fig. 13A

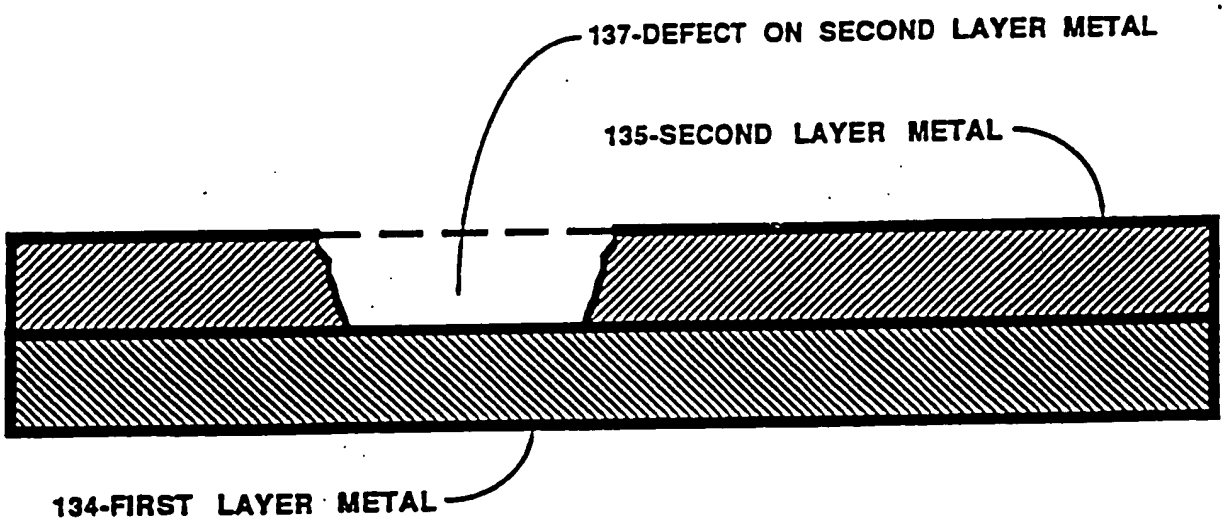



Fig. 13B

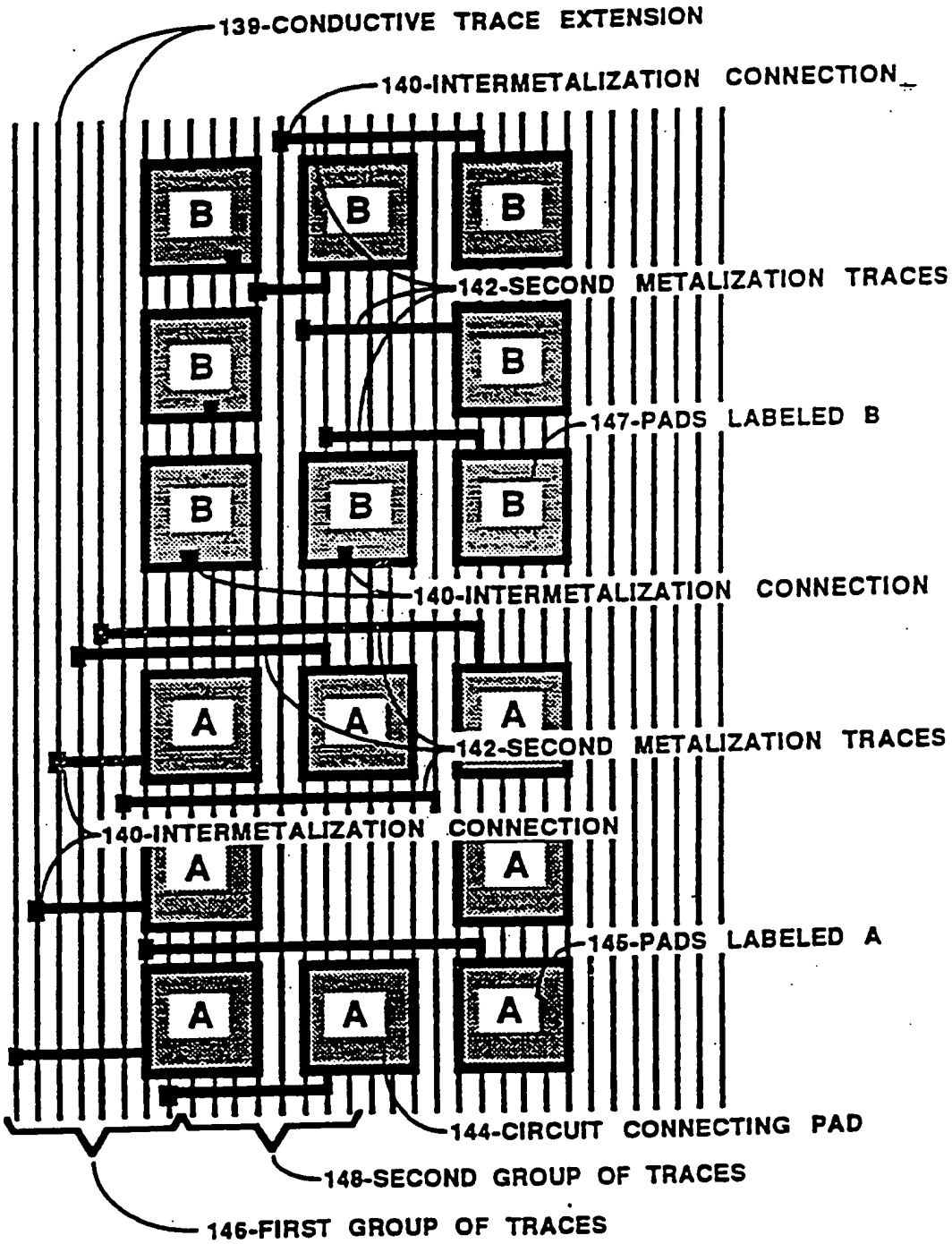

138-CONDUCTIVE TRACE EXTENSION
140-INTERMETALIZATION CONNECTION
142-SECOND METALIZATION TRACES
147-PADS LABELED B
140-INTERMETALIZATION CONNECTION
142-SECOND METALIZATION TRACES
140-INTERMETALIZATION CONNECTION
145-PADS LABELED A
144-CIRCUIT CONNECTING PAD
148-SECOND GROUP OF TRACES
146-FIRST GROUP OF TRACES
B
A

Fig. 14A

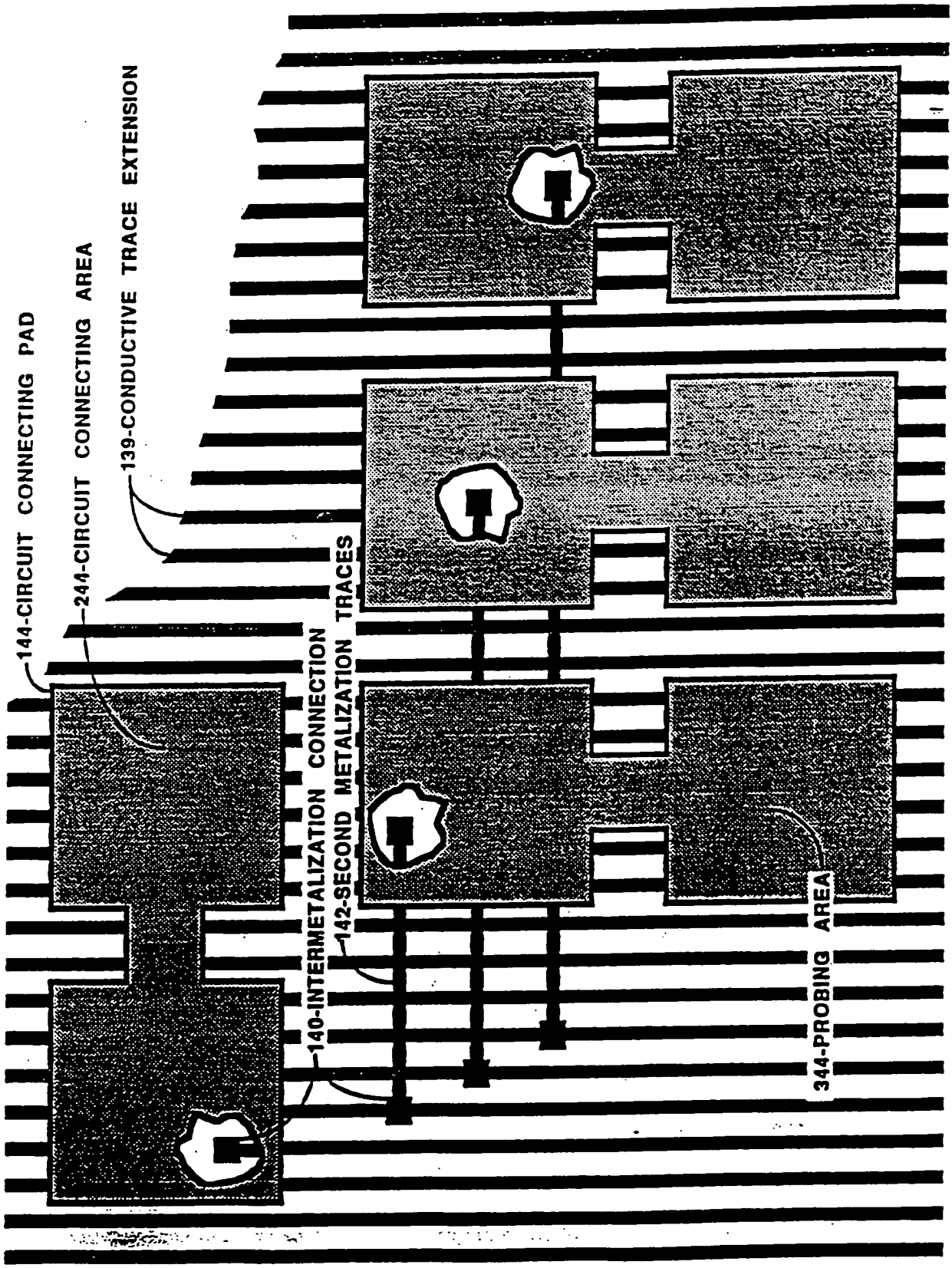

144-CIRCUIT CONNECTING PAD
244-CIRCUIT CONNECTING AREA
139-CONDUCTIVE TRACE EXTENSION
140-INTERMETALIZATION CONNECTION
142-SECOND METALIZATION TRACES
344-PROBING AREA

Fig. 14B

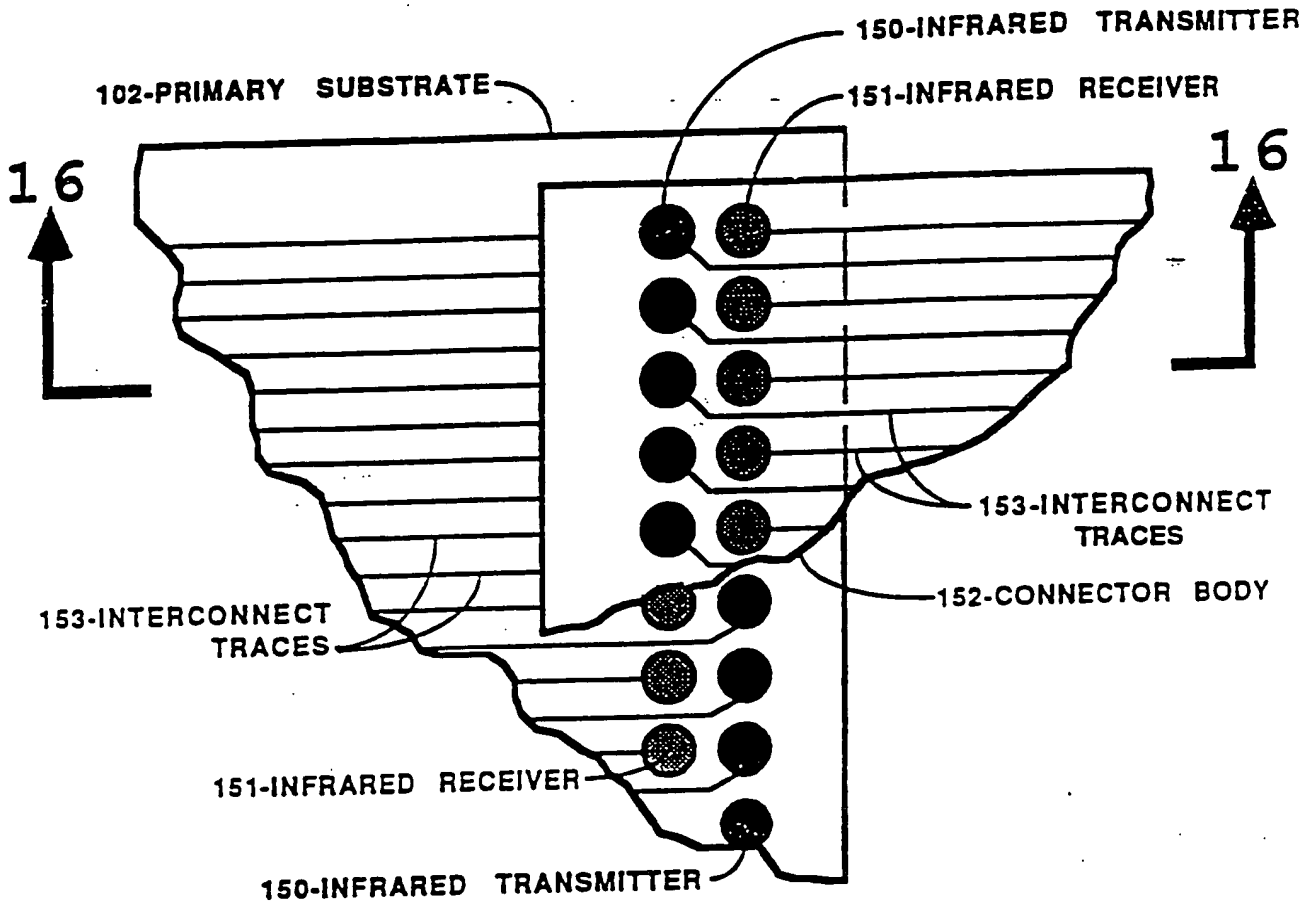

150-INFRARED TRANSMITTER
102-PRIMARY SUBSTRATE
151-INFRARED RECEIVER
16
16
153-INTERCONNECT TRACES
152-CONNECTOR BODY
153-INTERCONNECT TRACES
151-INFRARED RECEIVER
150-INFRARED TRANSMITTER

Fig. 15

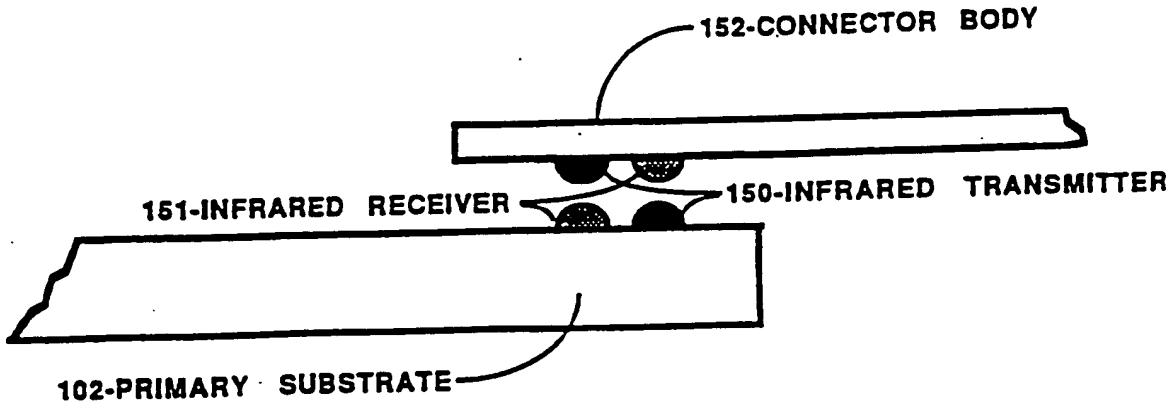

152-CONNECTOR BODY
151-INFRARED RECEIVER
150-INFRARED TRANSMITTER
102-PRIMARY SUBSTRATE

Fig. 16

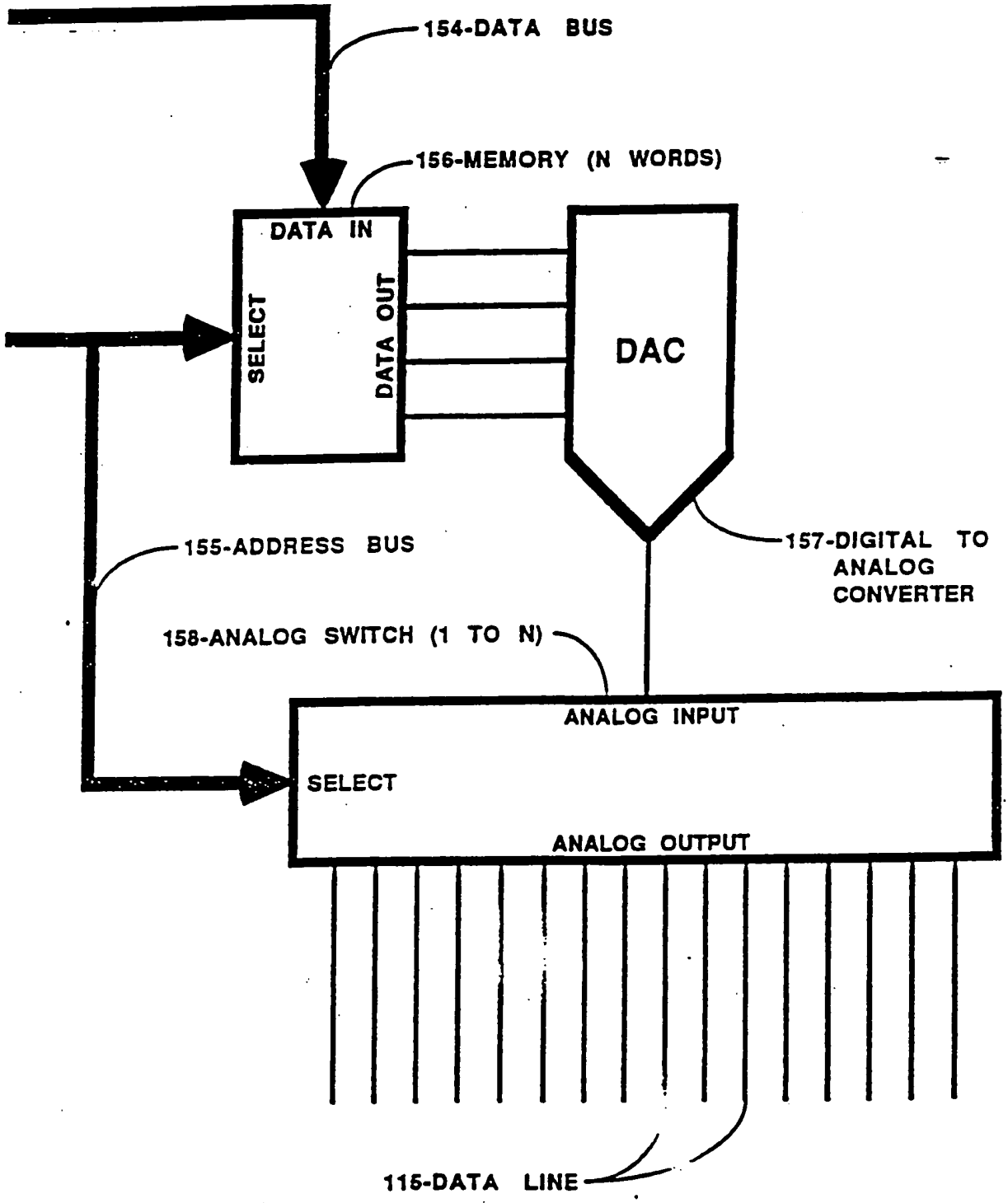

154-DATA BUS
156-MEMORY (N WORDS)
DATA IN
SELECT
DATA OUT
DAC
155-ADDRESS BUS
157-DIGITAL TO ANALOG CONVERTER
158-ANALOG SWITCH (1 TO N)
ANALOG INPUT
SELECT
ANALOG OUTPUT
115-DATA LINE

Fig. 17

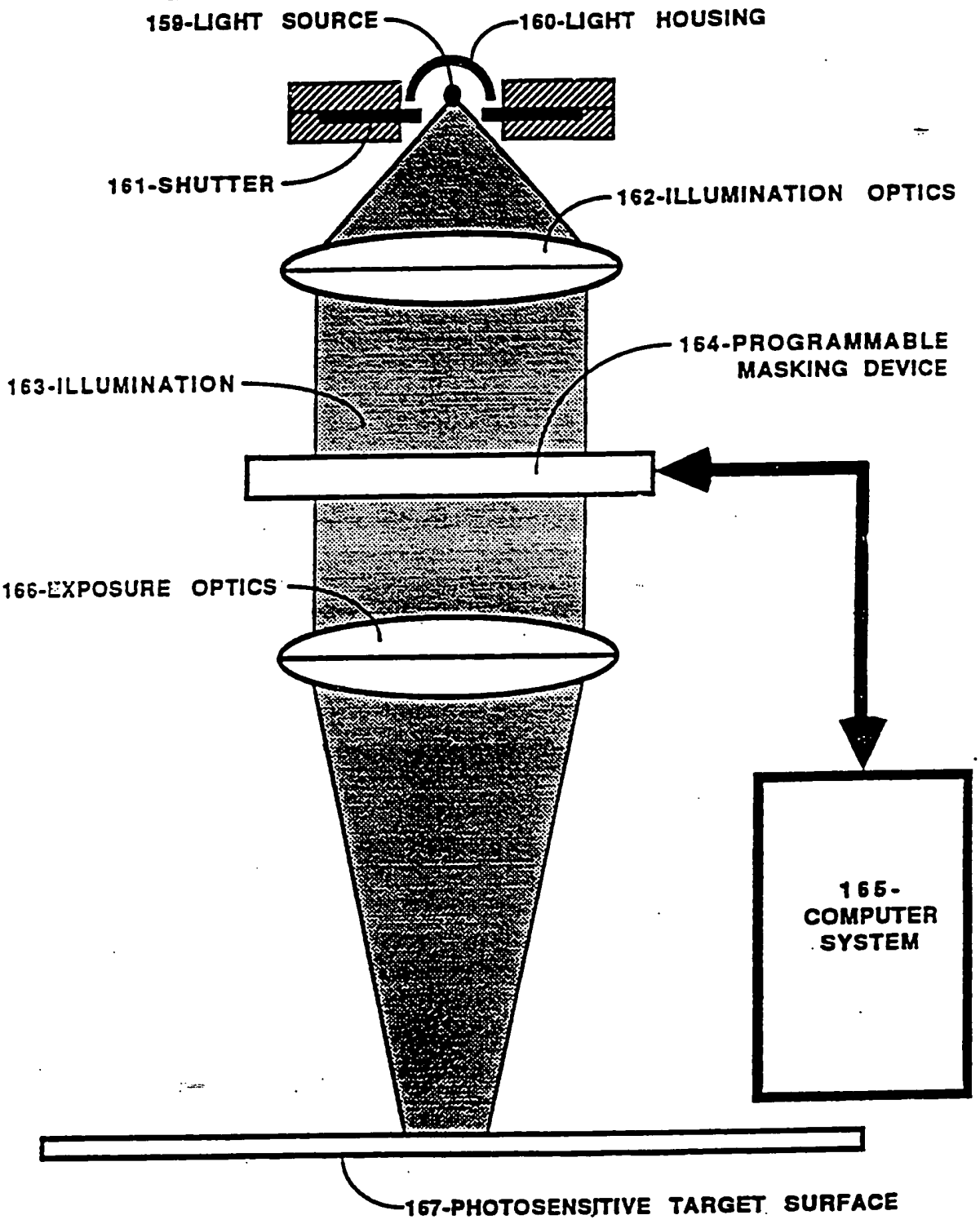

159-LIGHT SOURCE
160-LIGHT HOUSING
161-SHUTTER
162-ILLUMINATION OPTICS
163-ILLUMINATION
164-PROGRAMMABLE MASKING DEVICE
166-EXPOSURE OPTICS
165-COMPUTER SYSTEM
167-PHOTOSENSITIVE TARGET SURFACE

Fig. 18

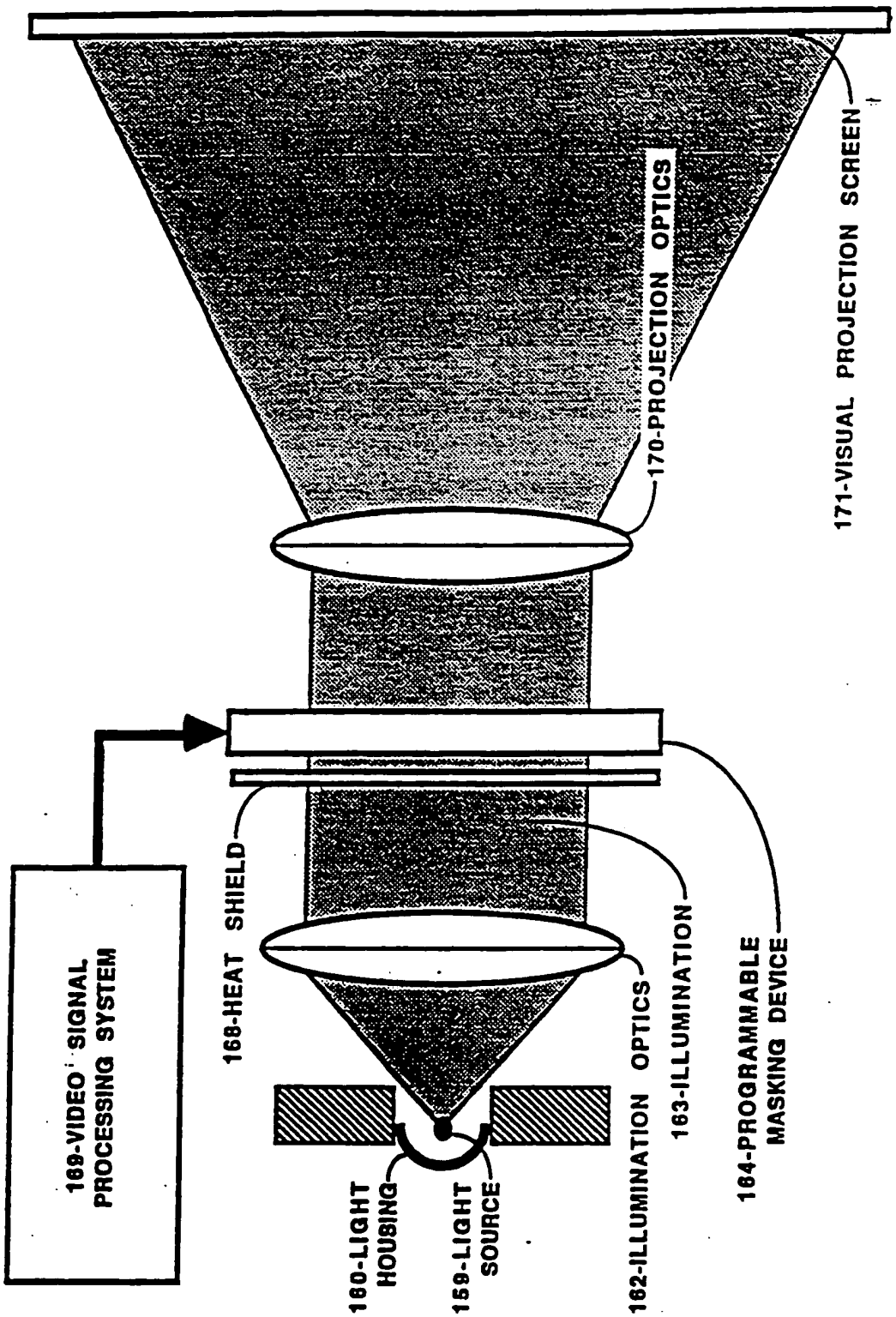

171-VISUAL PROJECTION SCREEN
170-PROJECTION OPTICS
169-VIDEO SIGNAL PROCESSING SYSTEM
168-HEAT SHIELD
163-ILLUMINATION
184-PROGRAMMABLE MASKING DEVICE
162-ILLUMINATION OPTICS
160-LIGHT HOUSING
159-LIGHT SOURCE

Fig. 19

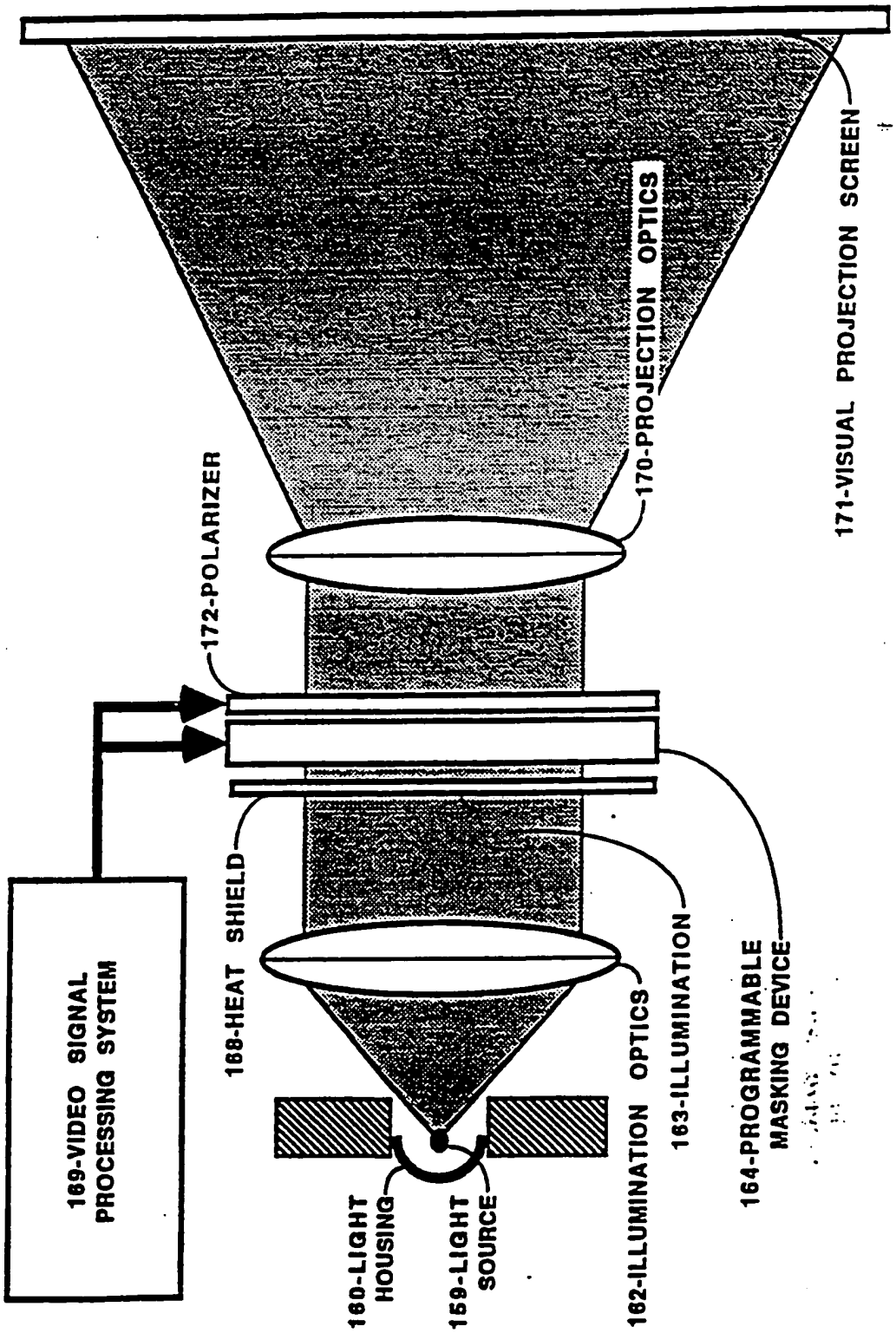

171-VISUAL PROJECTION SCREEN
170-PROJECTION OPTICS
172-POLARIZER
168-HEAT SHIELD
164-PROGRAMMABLE MASKING DEVICE
163-ILLUMINATION OPTICS
162-ILLUMINATION
160-LIGHT HOUSING
159-LIGHT SOURCE
169-VIDEO SIGNAL PROCESSING SYSTEM

Fig. 20

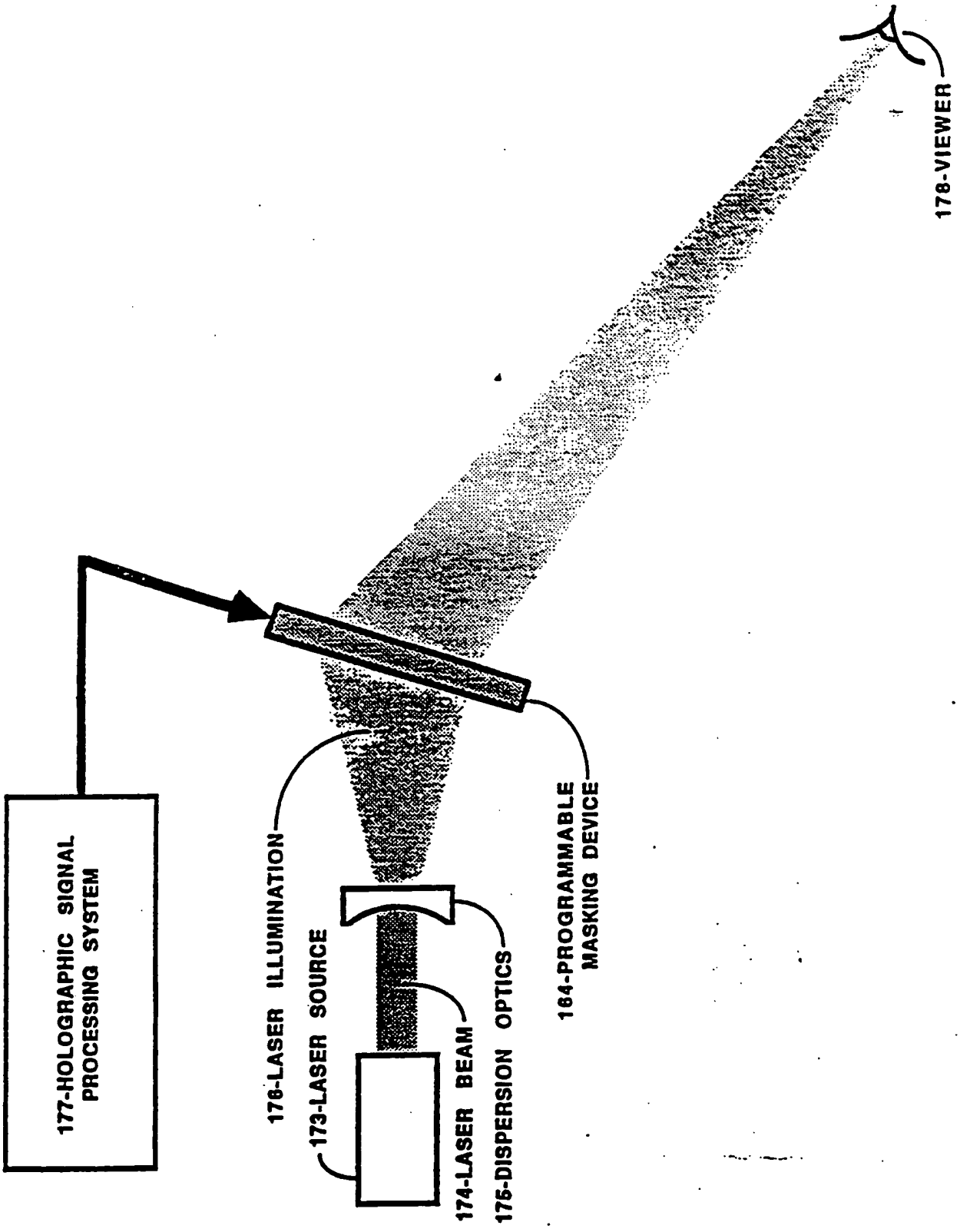

177-HOLOGRAPHIC SIGNAL PROCESSING SYSTEM
176-LASER ILLUMINATION
173-LASER SOURCE
174-LASER BEAM
175-DISPERSION OPTICS
184-PROGRAMMABLE MASKING DEVICE
178-VIEWER

Fig. 21

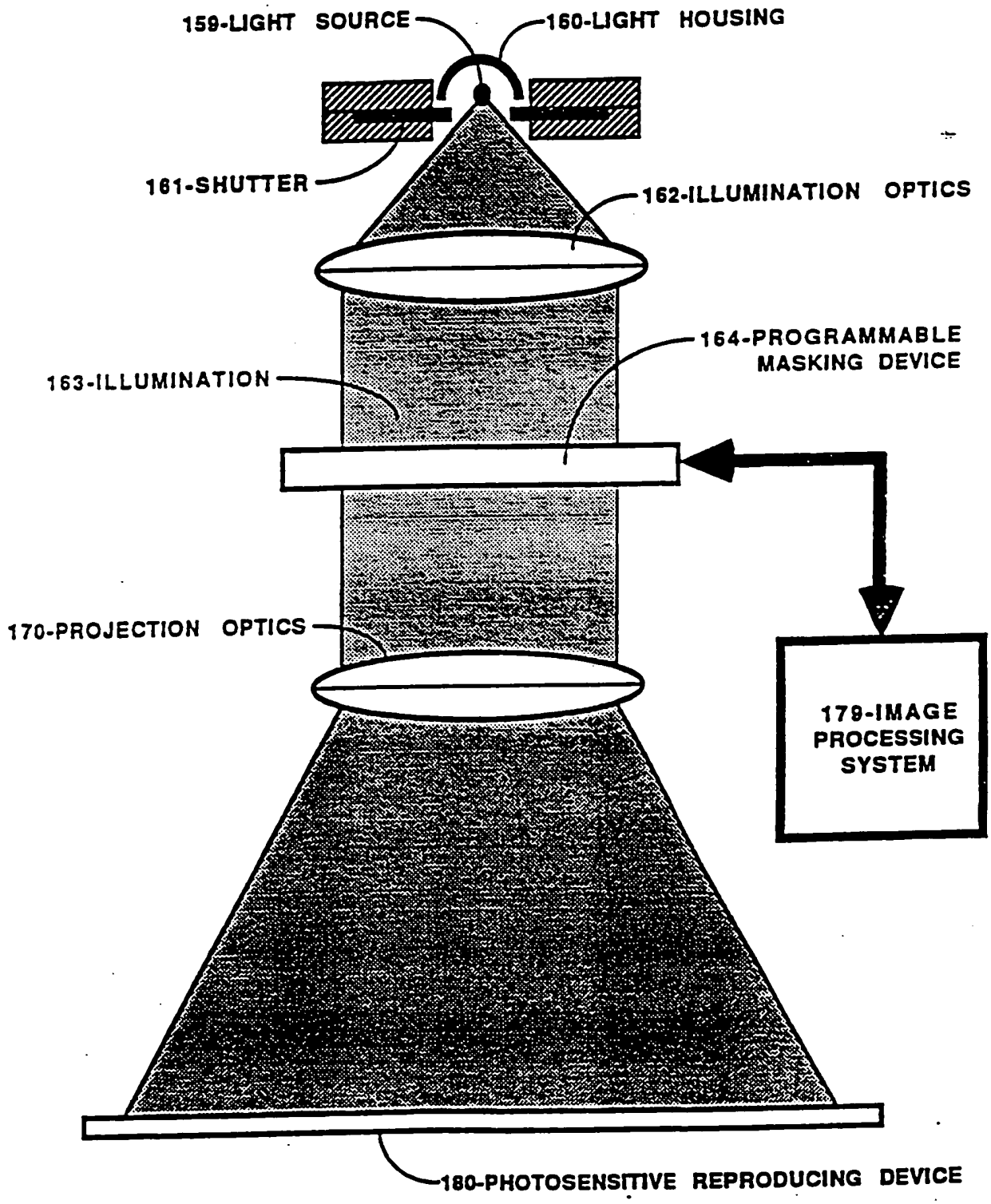

159-LIGHT SOURCE
160-LIGHT HOUSING
161-SHUTTER
162-ILLUMINATION OPTICS
164-PROGRAMMABLE MASKING DEVICE
163-ILLUMINATION
170-PROJECTION OPTICS
179-IMAGE PROCESSING SYSTEM
180-PHOTOSENSITIVE REPRODUCING DEVICE

Fig. 22

# INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/07331

## I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): G03F 9/00; C09K 19/00; G02F 1/13; G09G 3/36, 1/26

U.S. CL; 430/5, 20; 350/333, 331R; 340/784, 795

## II. FIELDS SEARCHED

Minimum Documentation Searched [4]

| Classification System | Classification Symbols |
|---|---|
| U.S. | 430/5, 20; 340/784, 795; 350/333, 331R; 428/1 |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [5]

## III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

| Category * | Citation of Document, [16] with indication, where appropriate, of the relevant passages [17] | Relevant to Claim No. [18] |
|---|---|---|
| X<br>Y | US, A, 4,653,860 (HENDRIX)<br>31 MARCH 1987; See entire document. | 1-6,15-17,20-35,46<br>7-14,36-45 |
| Y, P | US, A, 4,944,578 (DENTSON)<br>31 JULY 1990; See entire document. | 1-17, 20-46 |
| Y | US, A, 4,013,466 (KLAIBER)<br>22 MARCH 1977; See entire document. | 1-17, 20-46 |
| Y | US, A, 4,807,973 (KAWASAKI)<br>28 FEBRUARY 1989; See entire document. | 4,9-13,18-19,37-39 |
| Y | US, A, 4,840,459 (STRONG)<br>20 JUNE 1989; See entire document. | 4,9-13,18-19,37-39 |
| A | US, A, 4,723,838 (AOKI)<br>09 FEBRUARY 1988; See entire document. | 1-46 |
| A, P | US, A, 4,963,001 (MIYAJIMA)<br>16 OCTOBER 1990; See entire document. | 1-46 |
| A | US, A, 4,810.060 (UKAI)<br>07 MARCH 1989; See entire document. | 1-46 |

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

## IV. CERTIFICATION

| Date of the Actual Completion of the International Search [2] | Date of Mailing of this International Search Report [2] |
|---|---|
| 06 FEBRUARY 1991 | 19 MAR 1991 |

| International Searching Authority [1] | Signature of Authorized Officer [20] |
|---|---|
| ISA/US | Thomas R. Neville |

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . because they relate to subject matter [1] not required to be searched by this Authority, namely:

2. ☐ Claim numbers . because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [1], specifically:

3. ☐ Claim numbers_____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application, as follows:

See Attached Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☒ No protest accompanied the payment of additional search fees.

ATTACHMENT TO FORM PCT/ISA/210 (SUPPLEMENTAL SHEET 2) SECT VI

Group I. Claims 1-17 and 20-32 drawn to an imaging system which employs a programmable masking device and a method of using, classified in Class 430, Subclass 5 which have been included together because they possess unity of invention under PCT Rule 13.

Group II. Claim 18 drawn to a method for testing the integrity of transistor switches classified in Class 350, Subclass 331R. The inventions of Groups I and II are related as process of making and product made. The method of Group II can be used to make a materially different product such as a liquid crystal display device. Applicant has provided no evidence that the transistor switches of the Group I system cannot be tested using methodology other that set forth in Group II. Groups I and II are lacking unity under PCT Rule 13.

Group III. Claim 19 drawn to a method for substituting switch connectors classified in Class 350, Subclass 333. The inventions of Groups III and I are related as process of making and product made. The method of Group III can be used to make a materially different product such as a liquid crystal display device. Applicant has provided no evidence that Group III method of effecting switch connection substitutions cannot be performed by other well known in the art techniques. Groups III and I are lacking of unity under PCT Rule 13.

Group IV. Claims 33-46 drawn to a method of providing a masking device classified in Class 350, Subclass 333 and Class 340, Subclass 784. The inventions of Groups IV and Group I are related as a process of making and a product made. The product of Group I can be made using art recognized methods otehr than those specifically deleneated in Group IV. Applicant has provided no evidence that the particular steps specified in Group IV are critical to producing the imaging system of Group I. Groups IV and I are lacking of unity under PCT Rule 13.